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THESIS

COMPOSITE OPERATIONAL AMPLIFIERS AND THEIR USE IN IMPROVING BANDWIDTH, SPEED AND ACCURACY IN ACTIVE NETWORKS

by

Michael A. Luczak

June 1985

Thesis Advisor: Sherif Michael

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This research examines a unified approach to several of the problems associated with Operational Amplifiers(OAs), namely, speed, accuracy, and frequency dependent gain. The approach which is examined is the Composite Operational Amplifier(CNOA), where N=2, 3, or 4 single OAs. The CNOA is found to greatly extend the useful operating frequencies of the OA while maintaining low sensitivity to circuit element variations and a high degree of stability. It also provides a method for obtaining a fast and accurate OA. An additional feature of the CNOA is that it can be implemented using current technology. A computer model for the single OA was created and validated, and provided the basis for proving the superiority of the CNOA. Theoretical and exterimental results were used with these computer simulation results to fully substantiate the findings.

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Composite Operational Amplifiers and Their Use in Improving Bandwidth, Speed and Accuracy in Active Networks

by

Michael A. Luczak
Lieutenant Commander, United States Navy
B.S., SUNY College at Geneseo, 1968

Submitted in partial fulfillment of the
requirements for the degree of

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I. INTRODUCTION

A. BACKGROUND

The Operational Amplifier (OA) is used as the active element in most linear active circuits, namely, positive, negative, and differential gain amplifiers, integrators, and active filters. System design advancements have generated greater demands on the electrical performance of these OAs in several areas. These include extended bandwidth (BW), low sensitivity, and high stability, as well as high speed and high accuracy. Considerable research has ensued in an effort to improve the performance of the Operational Amplifier. Their non-ideal performance introduces frequency dependent gains which limit the operating frequencies of the linear active circuits which employ them. The effect of this non-ideal behavior actually contributes somewhat less to the BW limitation problem than the effect of the passive components associated with the circuits. Thus, if the ideal mathematical model input-output relationship is $H_i(s)$, then the actual circuit yields $H_a(s)$, which is different from $H_i(s)$. Further variations in $H_a(s)$ result from changes in frequency, temperature, and power supply voltage. A discussion of recent efforts to minimize these variations is contained in Section C of this chapter.

The requirement to improve the speed (slew rate) and accuracy (offset) of OAs has been driven by such applications as the introduction of the 16 bit analog-to-digital (A/D) and digital-to-analog (D/A) converters. The general results of efforts to improve these characteristics of OAs has been the attainment of greatly enhanced speed at the cost of a significant loss of accuracy. The slew rate of an OA is primarily determined by the type of input stage used, while the offset is determined by the imperfect match of the input stage transistors. A detailed discussion of the factors affecting the slew rate of an OA, as well as efforts to improve slew rate, is contained in Section D of this chapter.

This research proposes a new approach to extending the BW and improving the speed and accuracy of the OA. Each OA in a network is replaced by a Composite Operational Amplifier (CNOA), where N=2, 3, or 4, the number of single OAs required to achieve the realization. The resulting device has three terminals, consisting of an inverting input, a non-inverting input, and an output. Amplitude and phase compensation is accomplished by using resistor ratios as the controlling parameters. The CNOA has the same versatility as state-of-the-art designs using the same number of OAs, while at the same time maintaining the attractive features of the single OA, including low sensitivity to circuit element and power supply variations, as well as good stability. The investigation of the CNOA will consist of computer simulation, theoretical, and experimental analyses.

B. CHARACTERISTICS OF AN OPERATIONAL AMPLIFIER

This section will briefly discuss the characteristics of the OA. The OA is a three terminal Voltage Controlled Voltage Source (VCVS), consisting of a positive (non-inverting), negative (inverting), and an output terminal. A simplified schematic for an OA is shown in Figure 1-1. If the non-inverting input is grounded and a signal is applied to the inverting input, the output will be 180 degrees out of phase with the input signal. If the inverting input is grounded and a signal is applied to the non-inverting input, the output will be in phase with the input signal. The amplified voltage is found at the output terminal. The differential open loop gain of the OA, denoted as A, is the gain of the OA with no feedback path, i.e., with none of the output referred back to the input. It is usually of the order of 10^5 or more.

It is useful to consider the OA as an "ideal" amplifier, and although in practice none of the ideal properties can be achieved, they can be approximated closely enough for most applications. Figure 1-2 shows the equivalent circuit of the ideal OA. The following properties are associated with the ideal OA shown in that figure:

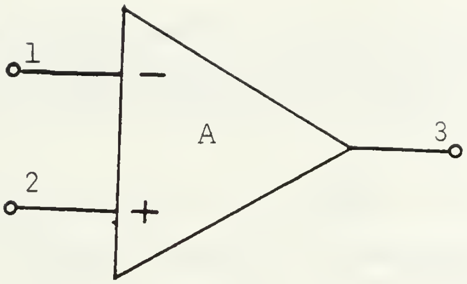


Figure 1-1 Schematic Diagram for a Simple OA

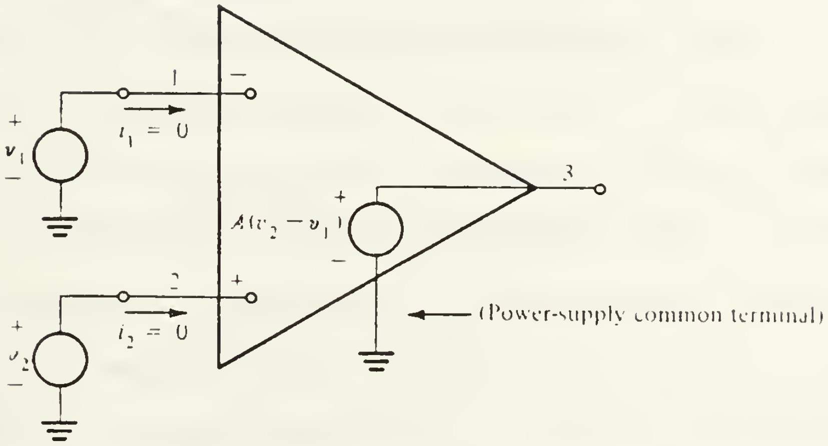


Figure 1-2 Equivalent Circuit of an Ideal OA

1. The ideal OA should not draw any current, i.e., the input current at terminal 1 and terminal 2 should be zero. This means that the ideal OA has infinite input impedance.

2. The output voltage between terminal 3 and ground should always be equal to $A(v_2-v_1)$, independent of the current drawn from terminal 3 into a load impedance. This means that the OA has zero output impedance.

3. The OA responds to a different voltage, v_2-v_1, hence if $v_1=v_2$, then ideally the output will be zero. This property is known as common mode rejection and it is ideally infinite.

4. The open loop gain A is ideally infinite.

5. The open loop gain A remains constant from zero to infinite frequency, i.e., it amplifies all frequencies equally.

The operational amplifier is a multistage amplifier. Figure 1-3 shows a basic three stage OA. The first stage of this OA is a differential amplifier which provides high gain to difference signals, v_2-v_1, and low gain to common-mode signals. The differential amplifier also sets the input impedance and its characteristics minimize the common-mode response and offset voltages. Offset voltages are small signals, usually on the order of a few millivolts, which cause some output voltage when $v_2-v_1=0$. They affect the accuracy of the OA and are caused by an imperfect match of the emitter-base voltages of the input transistors, Q1 and Q2. The second stage of the OA provides both current and voltage gain. The voltage gain contributes to the overall amplifier voltage gain and the current gain is used to drive the final stage without loading the input stage. The output stage of the OA

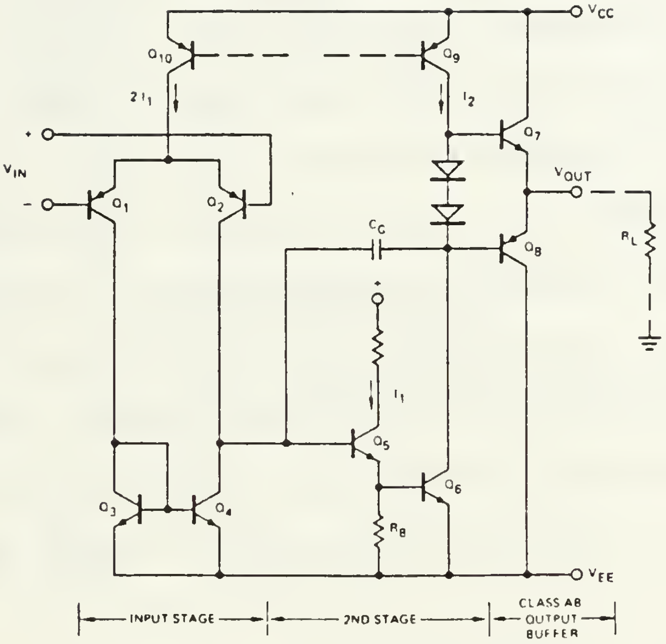


Figure 1-3 Typical Multistage OA

provides the amplifier with a low output resistance, corresponding to that of an ideal voltage source. Additionally, it must supply relatively large output currents without dissipating large amounts of power in the IC.

In practice, the differential open loop gain of an OA is finite and decreases with frequency. Although the gain is quite high at dc and low frequencies it starts to fall off at a relatively low frequency. Figure 1-4 shows the open-loop frequency and phase responses of a typical general-purpose, internally compensated OA. Internally compensated OAs usually utilize a single capacitor which gives a -20dB/decade rolloff(or, -6dB/octave). The constant -20dB/decade rolloff ensures stability of the OA. The gain of an internally compensated OA may be expressed approximately as

$$A(\omega) = \frac{A_o}{1 + j\omega/\omega_m} \qquad (1)$$

where A_o denotes the DC open loop gain and ω_m is the -3dB corner frequency (radians/sec). For $\omega >> \omega_m$, eqn. (1) becomes

$$A(\omega) \simeq \frac{A_o \omega_m}{j\omega} \qquad (2)$$

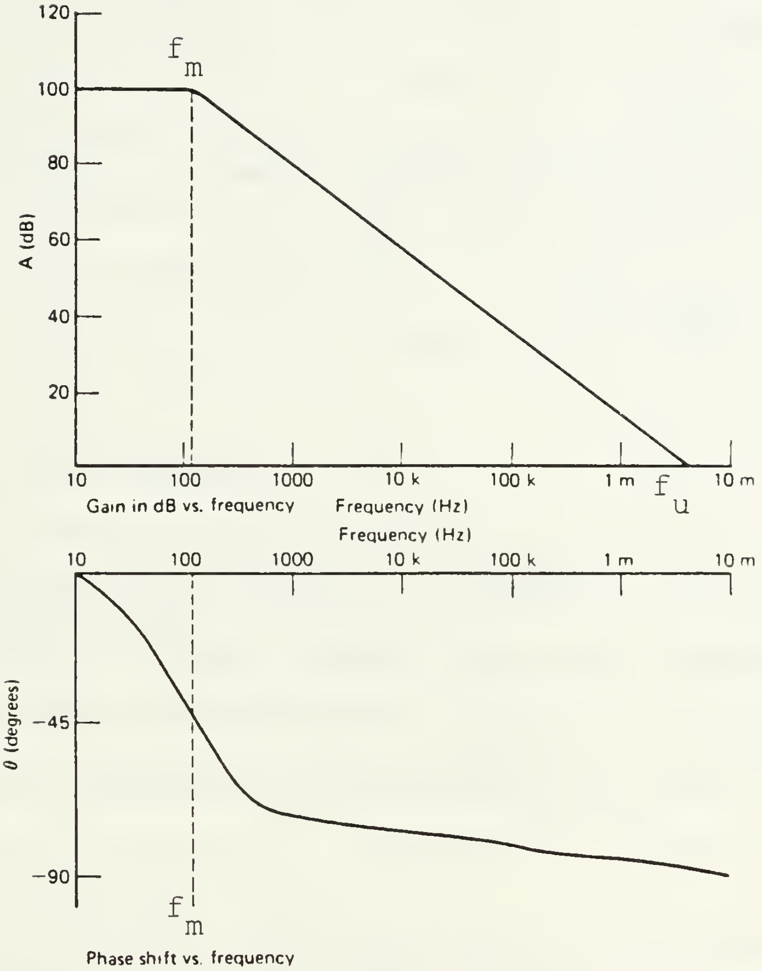


Figure 1-4 Open Loop Frequency and Phase Responses for a Typical Internally Compensated OA

and thus the frequency where the gain A_o reaches unity (0 dB), ω_u, is given by

$$\omega_u = A_o \omega_m \tag{3}$$

Substituting eqn. (3) into (2) gives

$$A(\omega) = \frac{\omega_u}{j\omega} = \frac{f_u}{jf}$$

where $f_u = \omega_u/2\pi$.

The term ω_u (rad/sec) or f_u (Hz) is known as the unity gain bandwidth (or, gain bandwidth product (GBWP)). In the simple OA, f is limited to approximately 1 MHz [Ref. 1]. This limitation is imposed by the requirement to limit the phase in excess of 90 degress.

C. OPERATIONAL AMPLIFIER BANDWIDTH

The high frequency rolloff of the OA imposes a limitation on the useful frequency range of linear active circuits. As discussed in Section A of this chapter, further practical limitations on the useful bandwidth of the OA are imposed by passive circuit components, as well as variations in the temperature and power supply voltage. The following approaches to alleviate the BW problem have recently been considered by various researchers [Ref. 2: p. 4].

1. Passive Compensation

This approach includes introduction of additional passive components to produce an amount of phase lead to compensate for the phase lag due to the imperfect OA's. These passive components are adjusted for a specific temperature and power supply voltage to match the OA GBWPs. If the ambient temperature or power supply voltages change, adjustments of the components will be required. In addition to this impractical consideration, the precise GBWPs must be known.

2. Active Compensation

This approach adds an additional OA to complement each OA in a configuration. The additional OA has characteristics which closely match the first. Although this approach has been utilized for specific configurations, there has been no generalized method developed for application to all structures.

3. Wider GBWP OA's

In this approach wider GBWP OAs are utilized to replace existing OAs in an active network. Although this extends the useful operating frequency range of the OAs, these OAs are expensive to produce and their cost may not be justified when a large number is required.

In this research, the Composite Operational Amplifier (CNOA) will be shown to provide a unified approach for minimizing the effects of the variations described above and to extending the bandwidth of the OA. It will replace the simple OA in the active circuit and will utilize low cost OAs available with existing technology. In addition, the individual OAs which compose the CNOA do not require matched GBWPs.

Since much of this research is associated with the use of finite gain amplifiers, it is necessary to develop some basic relationships for this configuration. Figure 1-5 shows a schematic for the amplifier under consideration. This configuration is known as an inverting amplifier and as the mane implies the output is 180 degrees out of phase with the input. Since the positive terminal is at ground potential, the voltage at the input is given by $-V_o/A$. Thus, the current in R1 can now be found as

$$I_{R_1} = \frac{V_i-(-V_o/A)}{R_1} = \frac{1}{R_1}\left(V_i + \frac{V_o}{A}\right)$$

Since the OA has approximately infinite impedance and $I_{R_2} = I_{R_1}$, then the output voltage may be expressed as

$$V_o = -\frac{V_o}{A} - \frac{1}{R_1}\left(V_i + \frac{V_o}{A}\right) R_f$$

which simplifies to

$$\frac{V_o}{V_i} = \frac{-R_f/R_1}{1 + (1+R_f/R_1)/A} \qquad (4)$$

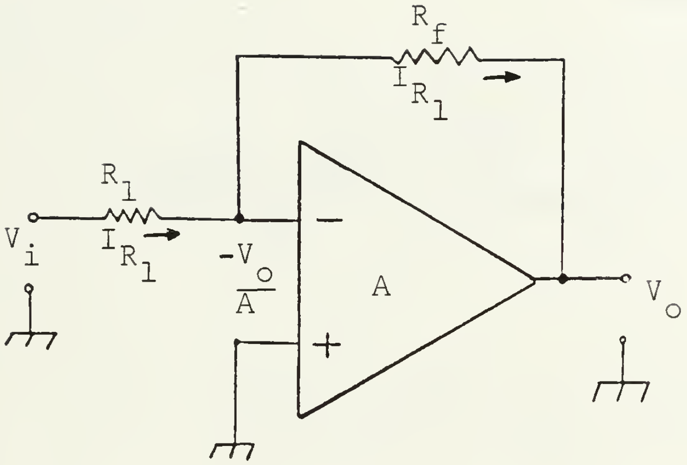


Figure 1-5 Schematic Diagram for an OA in an Inverting Configuration

As A approaches ∞,

$$\frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Using the open-loop frequency dependent expression given by eqn. (1) yields

$$\frac{V_o(\omega)}{V_i(\omega)} = -\frac{R_f/R_1}{1 + \frac{1}{A_o}(1 + \frac{R_f}{R_1}) + \frac{j\omega(1 + R_f/R_1}{\omega_u}}$$

For $A_o >> (1 + R_f/R_1)$, and from eqn. (3),

$$\frac{V_o(\omega)}{V_i(\omega)} \simeq -\frac{R_f/R_1}{1 + \frac{j\omega(1+R_f/R_1)}{\omega_u}}$$

These results show that the inverting configuration has a dc gain equal to $-R_f/R_1$, the ideal value. The closed-loop gain rolls off at a uniform -20 dB/decade slope with a 3 dB frequency given by

$$\omega_m = \frac{\omega_u}{1+R_f/R_1} \tag{5}$$

It can be shown by a similar analysis that the non-inverting amplifier has the same -20dB/decade rolloff, has a 3dB frequency also governed by equation (5), and has a dc gain of $(1 + R_f/R_1)$. These are very useful results and will be used later for analysis of the OA.

D. SLEW RATE LIMITATIONS

If an OA is overdriven by a large-signal pulse of a square-wave having a fast enough rise time, the output does not immediately follow the input. Figure 1-6 illustrates this response for a finite gain inverting amplifier. This response is known as the slew rate (SR) response and is defined as the maximum rate of change of the output voltage with respect to time. Figure 1-7 provides an effective model for calculating slew rate limits for an inverting amplifier. If the input to this amplifier is large enough to fully switch the differential amplifer, then the current $2I_1$ is directed to the integrator consisting of A and C. The SR is given by

$$SR = \left.\frac{dV_o}{dt}\right|_{max} = \frac{i_c(t)}{C}$$

and since $i_c(t)$ is always 2I, then

$$SR = \frac{2I_1}{C} \qquad (6)$$

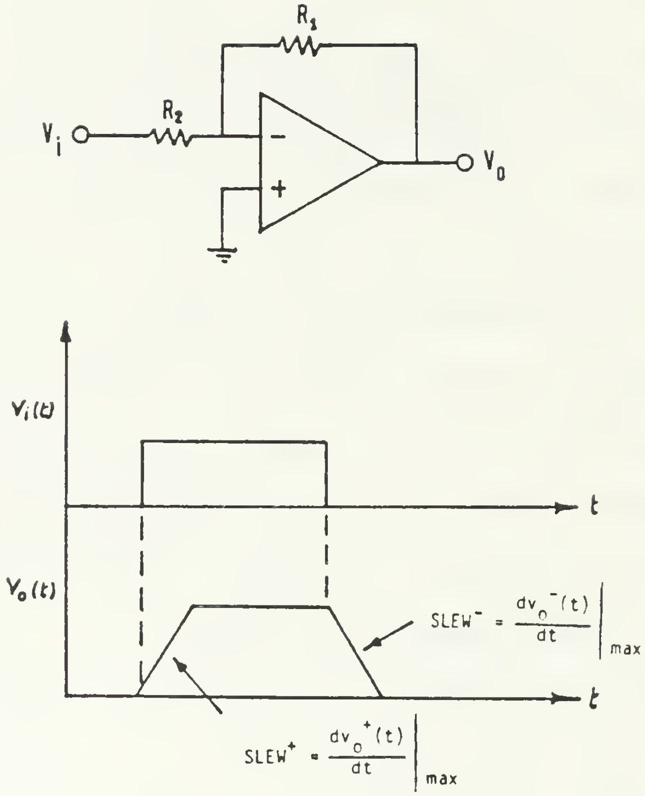


Figure 1-6 Large Signal "Slewing" Response Observed if the Input is Overdriven

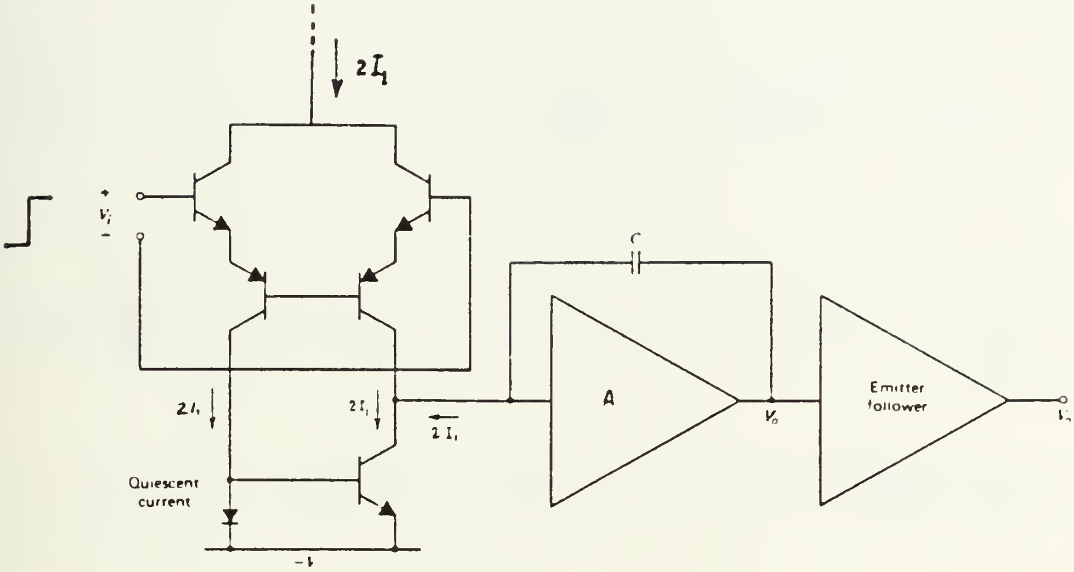


Figure 1-7 Model for Calculating Slew Rate Limits

Next, consider the small signal transconductance of the input stage, $gm_1 = I_1/V_i$. It follows that that the output voltage of the model shown in Figure 1-7 is given by

$$V_o(s) \simeq \frac{gm_1 V_i(s)}{sC}$$

that is,

$$A_v(\omega) = \left|\frac{V_o(\omega)}{V_i(\omega)}\right| = \left|\frac{gm_1}{\omega C}\right|$$

It follows that the open-loop unity gain frequency, ω_u, is given by

$$\omega_u = \frac{gm_1}{C} \tag{7}$$

Combining eqns. (6) and (7) above, the slew rate is given as

$$SR = \left.\frac{dV_o}{dt}\right|_{max} = \frac{2\omega_u I_1}{gm_1} \tag{8}$$

The above relationship is extremely useful. It shows that for a given GBWP, ω_u, the slew rate is determined totally by the ratio I_1/gm_1. Since ω_u is the point where excess phase begins to guild up, and since it is limited by technology rather than by circuit limitations, the only effective way to increase SR is to increase this ratio [Ref. 3].

Full-power bandwidth may be defined as the maximum frequency at which the full output swing can be obtained without distortion [Ref. 4]. If the output signal of an OA circuit is equal to $V_o = V_p \sin\omega t$, then

$$\frac{dV_o}{dt} = \omega V_p \cos \omega t$$

and,

$$SR = \left.\frac{dV_o}{dt}\right|_{max} = \omega V_p \qquad (9)$$

Thus, the highest frequency that can be reproduced without distortion is

$$\omega_{max} = \frac{1}{V_p} \left.\frac{dV_o}{dt}\right|_{max} \qquad (10)$$

From the relationship above it can be seen that SR and power bandwidth are related by the inverse peak of the sine wave, V_p. Figure 1-8 shows the distortion which results if an attempt is made to amplify a sine wave with $\omega > \omega_{max}$. In practical terms this means that for an LM741, whose maximum slew rate is limited to approximately 0.67v/μsec [Ref. 5],

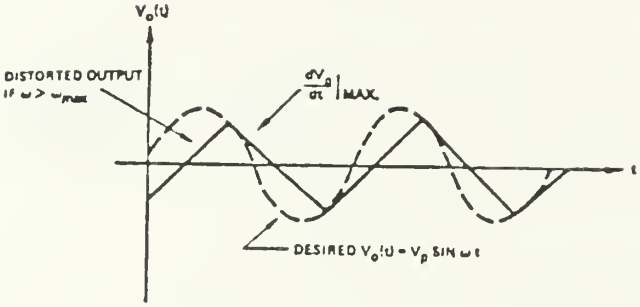

$V_o(t)$
DISTORTED OUTPUT IF $\omega > \omega_{max}$
$\frac{dV_o}{dt}\Big|_{MAX}$
t
DESIRED $V_o(t) = V_p \sin \omega t$

Figure 1-8 Slew Rate Limiting Effects on Output Sinewave that Occur if Frequency is Greater than Power Bandwidth

the maximum undistorted output frequency for a 10 volt peak output, the power bandwidth, is

$$f_{max} = \frac{SR}{2\pi V} = \frac{0.66x10^6}{2\pi x10} = 10.66 \text{ kHz}$$

This is a relatively low frequency compared with the bandwidth available using the 741 OA and clearly indicates the need for a higher slew rate OA.

E. METHODS FOR INCREASING SLEW RATE

Several methods have been utilized to improve the slew rate performance of operational amplifiers and are presented below.

1. Increasing the Ratio I_1/gm_1

From the previous section, equation (8) shows that the slew rate of an OA can be improved by increasing the ratio I_1/gm_1. One way to do this is by the addition of emitter degeneration resistors in the input stage, as shown in Figure 1-9. It can be shown that the slew rate can be increased by a factor of $(1 + gm_1R_E/2)$ [Ref. 4]. This effect can be observed in the LM 118, where a twenty-fold increase over similar OA's with no emitter resistors is achieved. There are problems associated with this method however. Unless the resistors are extremely well-matched, they contribute to increased input offset voltage and drift. Additionally, the thermal noise of the resistors degrades noise performance of the OA.

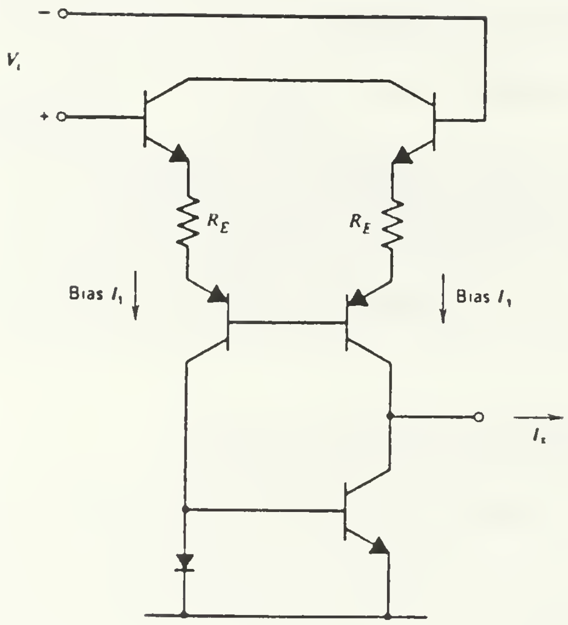


Figure 1-9 Inclusion of Emitter Degeneration Resistors in the Input Stage of Typical OA in Order to Improve the Slew Rate

2. Utilizing Field Effect Transistors(FET's)

The FET(JFET or MOSFET) has considerably lower transconductance than a bipolar device. Utilizng FETs in the input stage of an OA makes use of this normally considered "poor" feature of these devices and provides slew rate enhancement of the amplifier. This enhancement results from an adjustment of the ratio of equation (8). Figure 1-10 shows a model with JFETs in the input stage. It can be shown that the JFET slew rate is greater than that achieved by utilizing Bipolar Junction Transistors (BJTs) in the input stage by a factor of $\approx \frac{V_T \omega_j}{(2kT/q)\omega_u}$, where ω_j and ω_u are the GBWPs for the JFET and BJT amplifiers, respectively, and V_T is the JFET threshold voltage. Thus, for a JFET threshold voltage of V_T = -2v and $\omega_j = \omega_u$, a slew rate increase of a factor of 40 can be achieved by use of JFETs in the input stage instead of BJTs. Further, if JFETs are substituted for all the slow pnp transistors of the OA circuit, GBWPs of a factor of ten times greater than that obtained by the use of BJTs are realized [Ref. 6]. From the relationship given above, the improvement factor in slew rate that can be obtained by substituting JFETs for BJTs can be approximated as

$$\approx \frac{2}{(2)(1.38\text{x}10^{-23})/(1.68\text{x}10^{-19})} \cdot \frac{10}{1} = 446$$

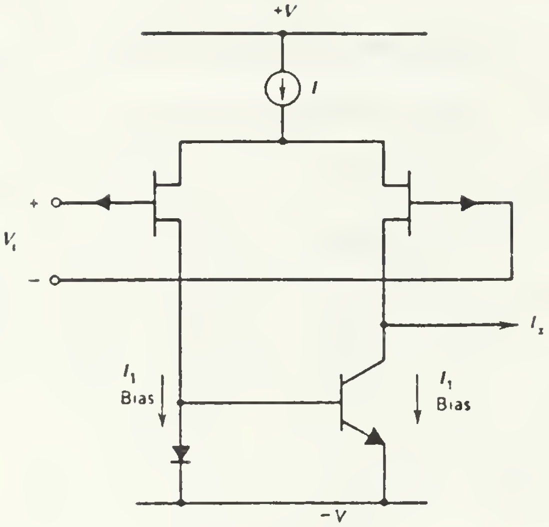


Figure 1-10 An OA Input Stage Using P-channel JFETs

Although this seems to offer an attractive method of slew rate enhancement, it is known to have an offset increase of three times greater than that of a BJT [Ref. 7].

3. Increasing the OA GBWP

For an OA with a simple differential input stage such as the one shown in Figure 1-3, the first stage transconductance is

$$gm_1 = \frac{q\ I_1}{kT}$$

and thus

$$\frac{gm_1}{I_1} = \frac{q}{kT}$$

Substituting the above expression into equation (8) gives

$$SR = \left.\frac{dV_o}{dt}\right|_{max} = \frac{2\omega_u kT}{q}$$

From this expression it can be seen that the slew rate of an OA with a simple differential input stage is a function of ω_u and some constants. Thus slew rate can be increased by increasing the corner frequency; but problems with excess phase can result unless an extremely good design is utilized. Although some good results have be obtained, it is questionable whether the difficulty of building such an OA is worth the improvement in slew rate achieved.

4. Increasing the Charging Current

This method of slew rate improvement results from an increase in charging current available to the compensating capacitor through alternative paths in the input stage. This method also finds limited application due to an increase in the offset voltage encountered.

E. CONCLUSIONS

This chapter has outlined some of the limitations associated with state-of-the-art OAs, including frequency dependent bandwidth, as well as speed and accuracy constraints. Methods to improve the OA bandwidth have been said to be deficient due to practical and/or economic considerations. It was shown that the current methods for slew rate enhancement result in an increase in offset voltage, as well as some degradation in noise performance in the case of the emitter resistor method. This research proposes the Composite Operational Amplifier (CNOA) as a unified approach to overcoming the limitations imposed by state-of-the-art Operational Amplifiers.

II. GENERATION OF AN OP AMP MODEL

A. BACKGROUND

Investigating the characteristics of the Composite Operational Amplifier (CNOA) by computer simulation required development of a single OA basic building block model. The OA selected for this model was the LM741. It was felt that this OA possesses the characteristics and degree of sophistication necessary to accurately and completely examine the operation of the CNOA. A schematic of the particular 741 selected is shown in Figure 2-1. The 741 was modelled using the computer program SPICE (Version 2G) which is resident on the IBM 3033 System.

B. THE SPICE PROGRAM

SPICE is a general-purpose circuit simulation program for linear AC, non-linear DC, and non-linear Transient Analyses [Ref. 8]. It is used extensively in the private sector as an analog and digital design tool. Circuits may be modelled which contain resistors, capacitors, inductors, independent voltage and current sources, dependent sources, and the four most common semiconductor devices: diodes, BJTs, JFETs, and MOSFETs.

Specific capabilities of SPICE which were particularly useful for this research include the following.

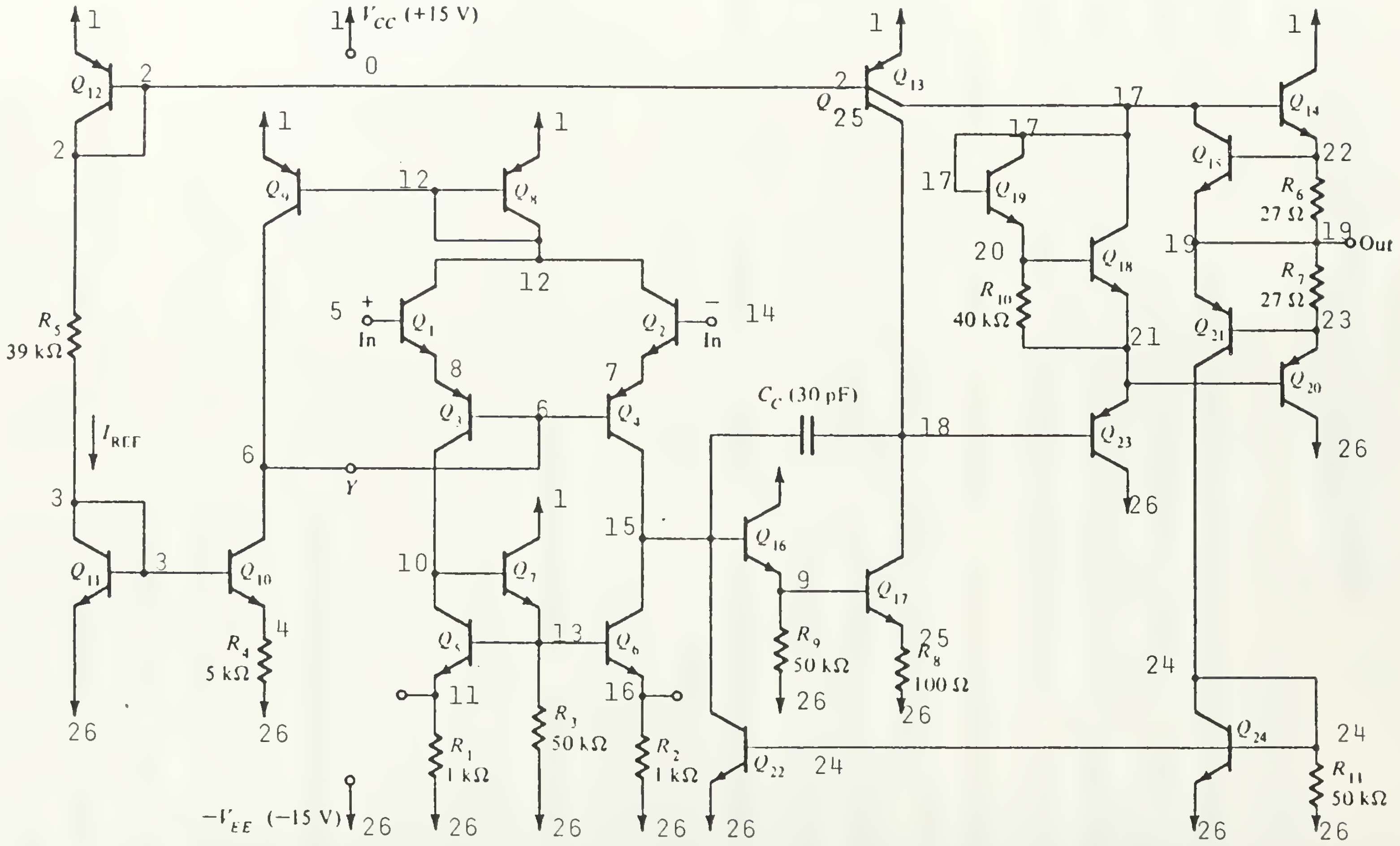


Figure 2-1 Schematic for Basic LM741 Computer Model

1. AC Analysis

The AC analysis capability of SPICE computes the AC output variables as a function of frequency. Initially, the DC operating point of the circuit is computed and the linearized small-signal models for all of the non-linear devices are created. The linearlized circuit is then analyzed over a user specified range of frequencies. The listing file for the SPICE program contains the DC nodal voltage values for the initial small signal bias solution, and if requested, a listing and plot of output values may be obtained. The AC analysis capability found specific application in determining OA and CNOA frequency and phase responses.

2. Transient Analysis

The transient analysis capability of SPICE computes the circuit response to a particular input over a user specified period of time. The initial transient conditions are automatically computed and are available in the listing file. Transient response data together with a plot of that data are available if requested. The transient analysis capability found specific application in determining OA and CNOA slew rate response.

3. DC Analysis

The DC analysis capability of SPICE automatically determines the linearized, small-signal model for non-linear devices if an AC analysis is requested and automatically determines the initial transient conditions if a transient analysis is requested. DC transfer curves may be generated by stepping an independent voltage source over a user specified interval. These curves and their associated data may be printed in the program's listing file if requested. The DC analysis capability found specific application in determining OA and CNOA offset characteristics as well as for circuit analysis. Detailed DC circuit analysis was greatly assisted through the use of ammeters in the circuitry.

The procedure for utilizing SPICE on the IBM 3033 system is relatively simple. First, a program is created in XEDIT utilizing the procedures of the SPICE Manual. Once the file is created SPICE may be entered by using the following commands:

```
CP LINK 0166p 191 192 rr
ACCESS 192 B
EXEC SPICEIT filename filetype
```

The file produced as a result of the execution of the above sequence is identified as RESULTS LISTING and may be used to analyze the circuit configuration.

C. OPERATION OF THE LM741

This section describes the operation of the OA selected as the simulation model and utilizes the schematic of Figure 2-1. This discussion follows that by Sedra [Ref. 9]. The circuit is designed with IC considerations in mind, that is, it utilizes a large number of transistors, relatively few number of resistors, and only one capacitor. These characteristics are dictated by limited silicon area, ease of component fabrication, and the quality of fabricated components. The OA normally operates with VCC=VEE=15V, however, it may operate at much lower voltages and still perform acceptably. Each section of the circuit and its basic operation are described below.

1. DC Bias Circuitry

The reference bias current for the OA, I_{REF}, is generated in the branch consisting of transistors Q11 and Q12, together with resistor R5. The bias current for the first stage is generated in the collector of Q10 through the current mirror formed by Q10, Q11, and R4. Transistors Q8 and Q9 also contribute to the biasing process. I_{REF} provides current to the double-collector lateral pnp transistor Q13/25. Transistors Q12 and Q13 form a two-port current mirror. The output from the collector of Q13 provides bias current to the output stage and the output from the collector of Q25 provides bias to Q17. Transistors Q18 and Q19 establish V_{BE} voltage drops between the bases of the output transistors Q14 and Q20.

2. Input Stage

The input stage consists of transistors Q1 through Q7, with biasing performed by Q8, Q9, and Q10. Transistors Q1 and Q2 act as emitter followers and establish a high amplifier input resistance, as well as delivering the differential input to the amplifier formed by Q3 and Q4. Transistors Q5, Q6, and Q7, together with resistors R1, R2, and R3 form a load for the input stage. The output of the input stage is taken from the collector of Q6. The transistors Q3 and Q4, in a common-base configuration, provide the OA with the ability to swing between positive and negative output voltages (called level shifting).

3. Intermediate Stage

The intermediate stage of the OA consists of transistors Q16, Q17, and Q25, together with resistors R8 and R9. Transistor Q16 acts as an emitter follower amplifier which gives the stage high input resistance, thus avoiding loading of the input stage. The high gain of the stage is accomplished without using a large load resistor, through the use of Q17 with an active load formed by Q25. Capacitor C_c is connected in the feedback stage to provide frequency compensation using the Miller compensation scheme. Capacitor C_c gives OA a dominant pole at approximately 5 Hz. Pole splitting causes the other non-dominant poles to be shifted to much higher frequencies and results in a uniform -20dB/decade rolloff and a GBWP approximately 1 MHz.

4. Output Stage

The purpose of the output stage of the OA is to provide the amplifier with low output resistance and to supply large load currents without dissipating unduly large amounts of power in the IC. The output stage is a Class AB output stage consisting of Q14 and Q20. This provides greater efficiency than an emitter follower stage would. Transistors Q18 and Q19 provide bias for the output stage. Transistor Q23 acts as an emitter follower, which minimizes the loading effect of the output stage on the second stage.

5. Short Circuit Protection

Short circuit protection in the LM741 is provided by transistors which conduct only if large amounts of current are drawn by the load. This would happen if the output terminal is short-circuited to one of the supply terminals. The short circuit protection circuitry consists of transistors Q15, Q21, Q22, and Q24, together with resistors R6 and R7.

D. GENERATION AND VALIDATION OF THE MODEL

A SPICE program was written utilizing the schematic of Figure 2-1 and the program is shown in Appendix A. Transistor parameter values for the 741 were determined from the literature [Refs. 9, 11], although most transistor values were not available and were allowed to default to SPICE assigned values. Nodes were added and node numbers were changed to accommodate the various configurations used in the research. Various analyses of the basic model were simulated and the results are summarized in Figure 2-2. Analyses performed to validate the model included the following:

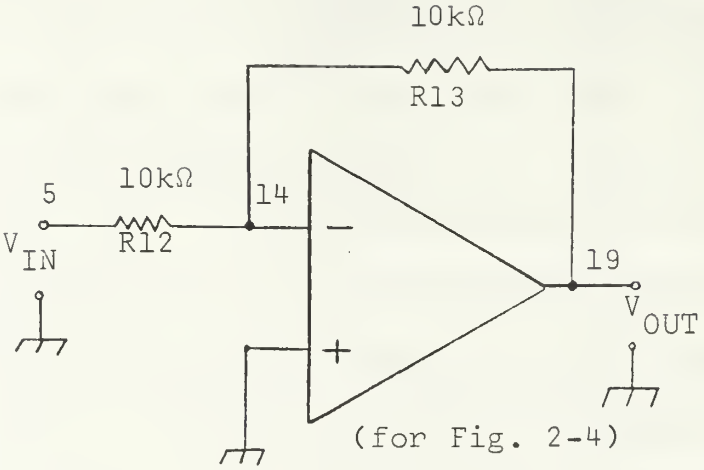
PARAMETER	MODEL VALUE	TYPICAL LM741
GBWP (MHz)	0.9	0.5-1.0
Slew Rate (V/μs)	±0.615	±0.6
V_{off}(mV)	0.15	1-5
I_{off}(nA)	0.14	3-200
Power Dissipated(mW)	49	50
-20 dB/decade rolloff		
Correct frequency and phase response		

TRANSISTOR	MODEL COLLECTOR CURRENT(μA)	THEORETICAL COLLECTOR CURRENT (μA)
Q1	9.6	9.5
Q2	9.6	9.5
Q12	736	730
Q13	177	180
Q14	531	550

Figure 2-2 Results of Analysis of LM741 Computer Model

1. The basic circuit was configured as both a positive (non-inverting) and negative (inverting) finite gain amplifier, with gains of k=10 and k= -10, respectively. An AC analysis of these amplifiers was performed by SPICE. The results showed a GBWP of 0.9 MHz and a constant -20 dB/decade rolloff. The output voltage agreed with theoretical values (i.e., $V_{OUT}(dB)=20\log(V_{OUT})$) and the proper phase response (showing a 45 degree phase shift at the dominant pole) was observed. Figure 2-3 shows schematics of the circuits used in these analyses and Figures 2-4 and 2-5 show the results. Appendices B and C show the programs used to generate these results.

2. A transient analysis of both the inverting and non-inverting amplifiers was simulated in a unity gain configuration. A large signal pulse (-5.0 to +5.0 volts) was input and a slew rate of ±0.615 v/usec was observed. This value is representative of a typical LM741. Some difficulty was encountered with the model at this point and should be mentioned. An unexplainable voltage spike was observed at the beginning of the leading edge of the response pulse for each configuration. Figure 2-6 shows this situation for the non-inverting configuration and Appendix D contains the computer program used to obtain these results. It is believed that this was due to the interaction of the specified values of the transistor junction capacitance with the defaulted values for the other transistor parameters



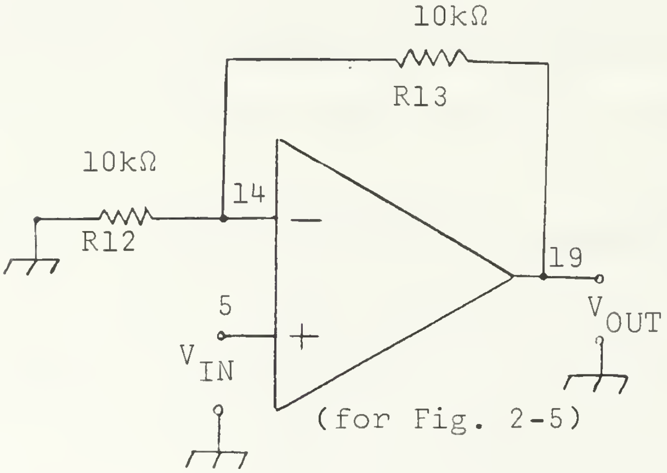


Figure 2-3 Schematics for Circuits Used for Frequency and Phase Response Analyses of Basic Computer Model

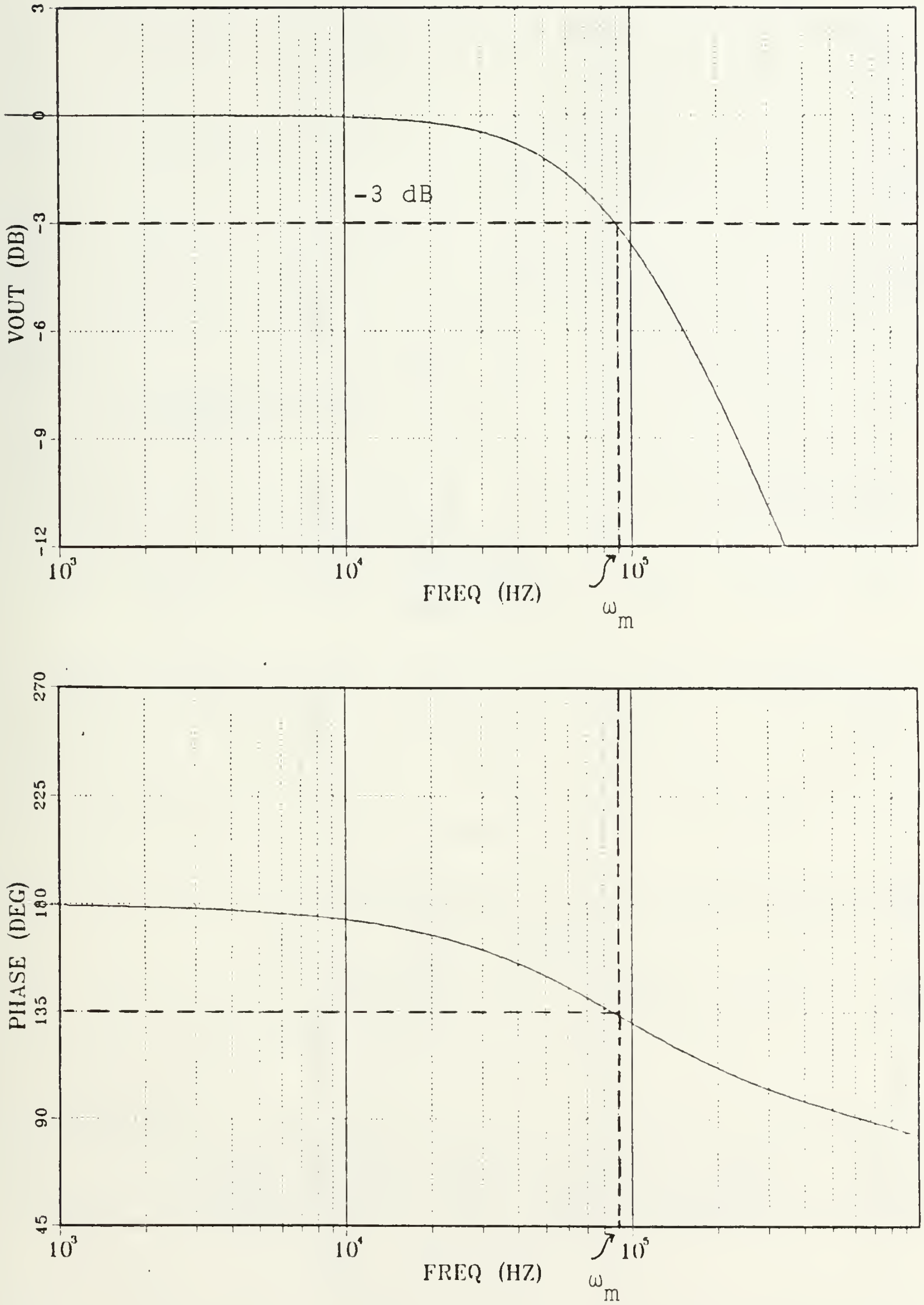


Figure 2-4 Frequency and Phase Response Curves for the Basic Model in an Inverting Configuration

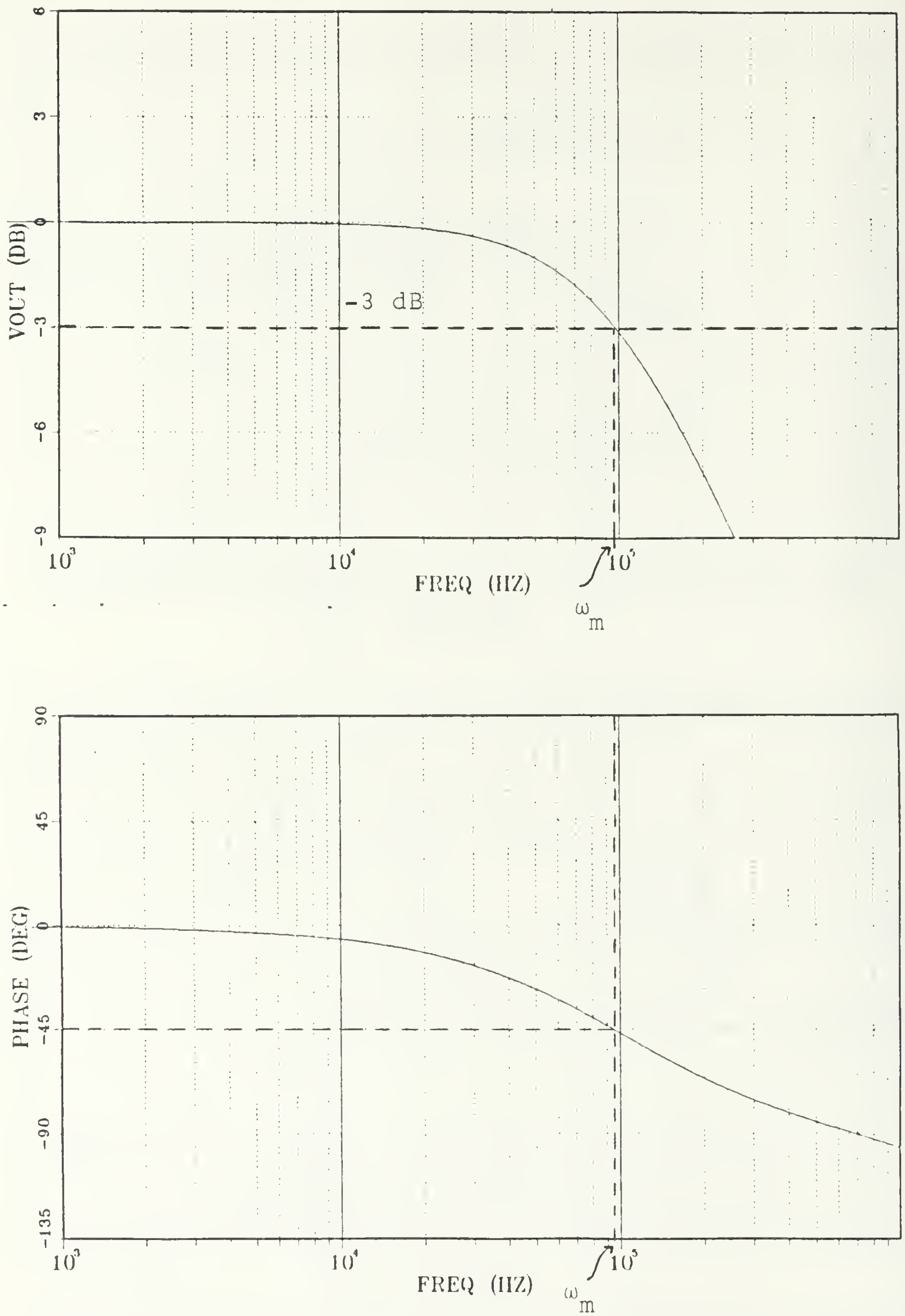
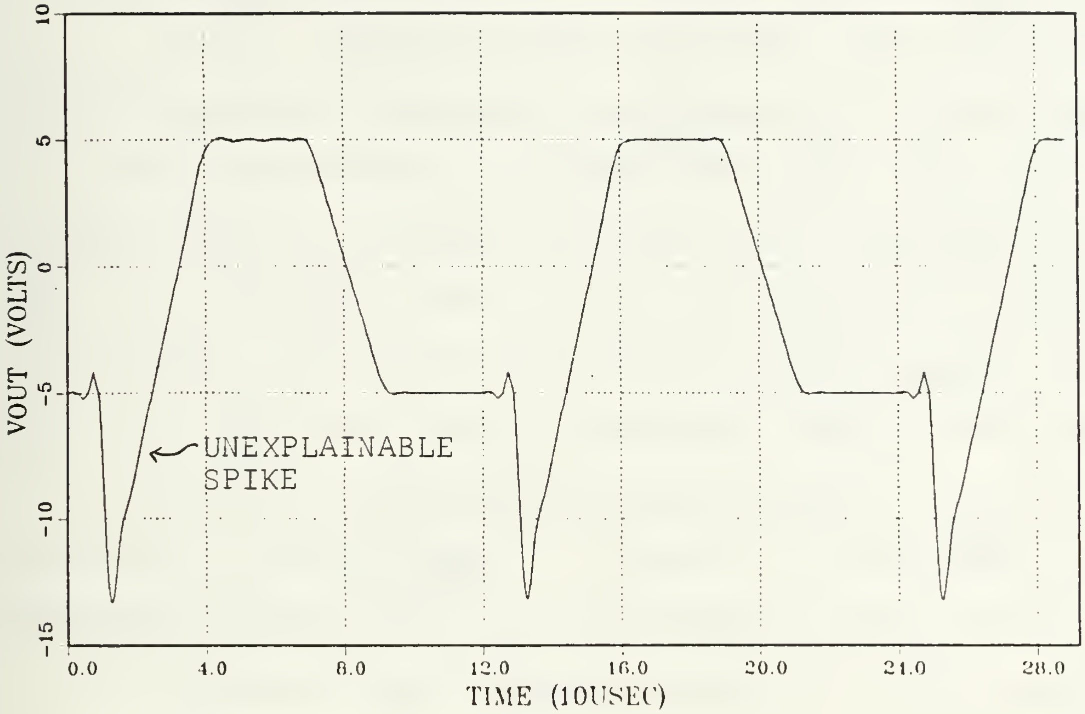


Figure 2-5 Frequency and Phase Response Curves for the Basic Model in a Non-Inverting Configuration



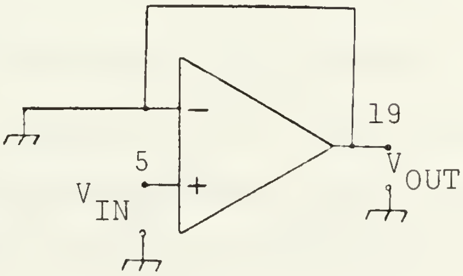


Figure 2-6 Slew Rate Results of Non-Inverting Configuration with Junction Capacitances Included in the Basic Model (Large Signal Response)

assigned by the system. These capacitances were included in the model in an effort to introduce the appearance of the second pole (which was never achieved). These capacitances were removed for all other slew rate analyses and the simplified model operated satisfactorily for these analyses. The model which contained the capacitances operated satisfactorily for all other analyses. The slew rate response curves are shown in Figure 2-7. Appendix E shows the programs utilized to obtain these results.

3. An AC analysis was performed to determine the open-loop gain of the model. A large resistor (93,600 kΩ) was used in the feedback path of a non-inverting amplifier configuration to simulate an open-loop situation. An open-loop gain estimate of 93,600 was obtained with the dominant pole appearing at 10.5 Hz. These values are considered to approximate those of an LM741. Figure 2-8 shows the plots of the results of this analysis and Figure 2-9 shows a schematic of the circuit used. Appendix F contain the program used in the analysis.

4. A DC analysis was performed to determine the collector currents of selected transistors in the model. Simulated and theoretical results compared very closely, as shown in Figure 2-2. Appendix G contains the program used in the analysis and Figure 2-10 shows a schematic of the circuit used in the analysis.

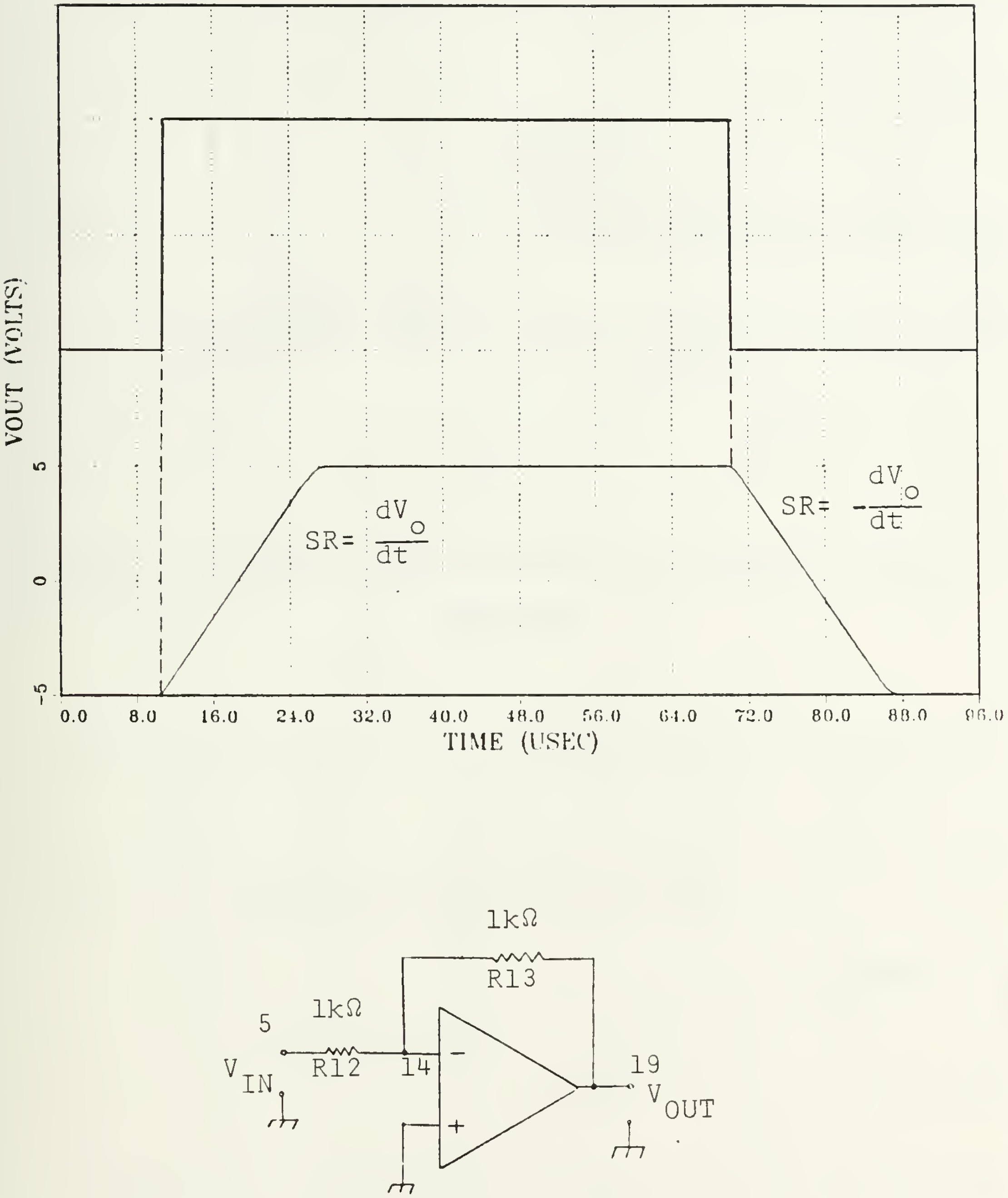


Figure 2-7 Large Signal Slew Response of Basic Model in Inverting Configuration

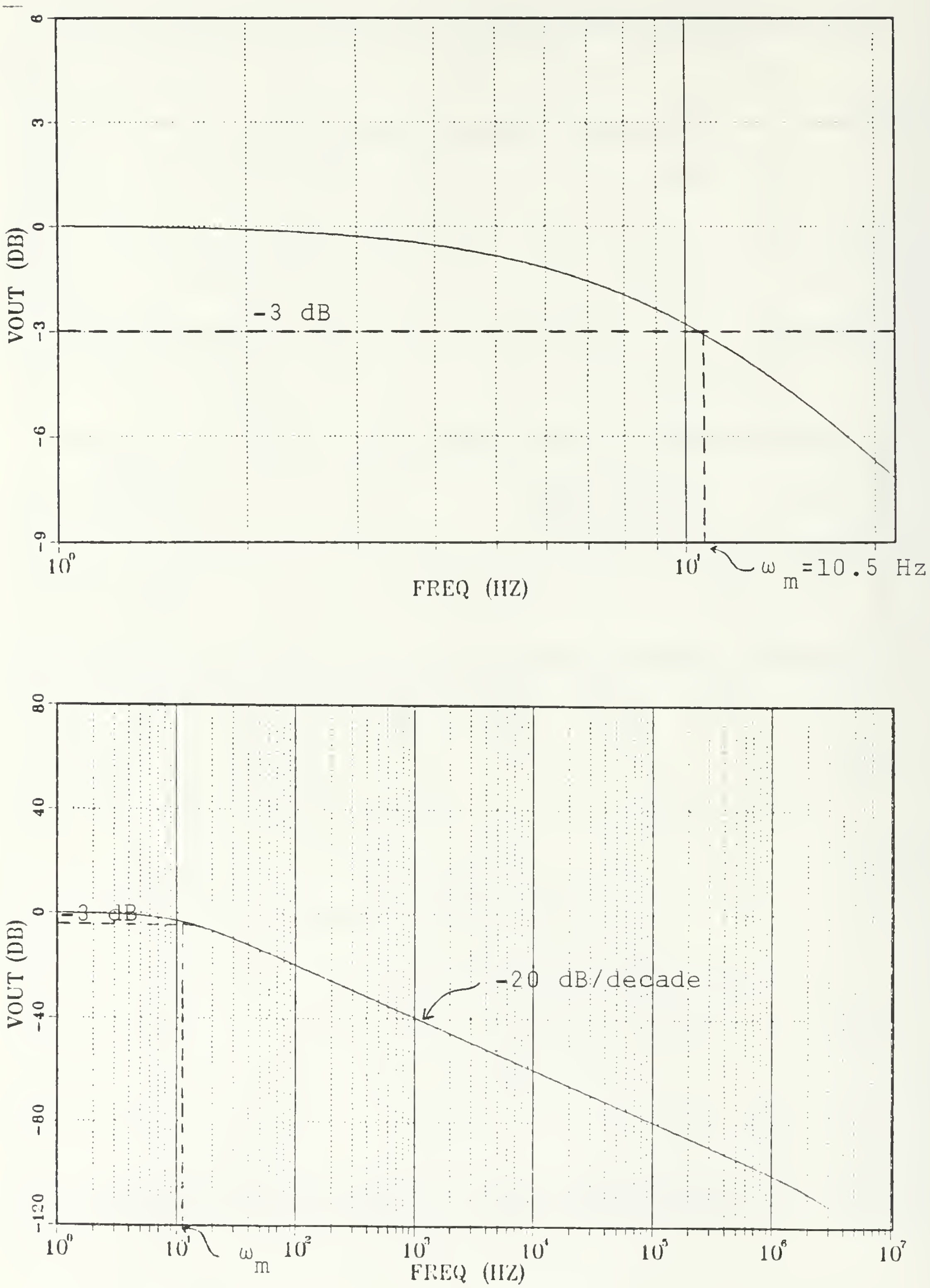


Figure 2-8 Open Loop Frequency Response Simulation of Basic Model

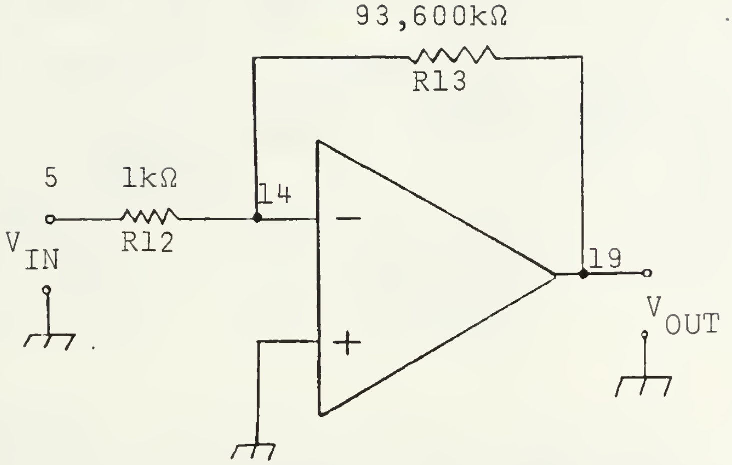


Figure 2-9 Schematic of Circuit Used for Open Loop Frequency Response Analysis

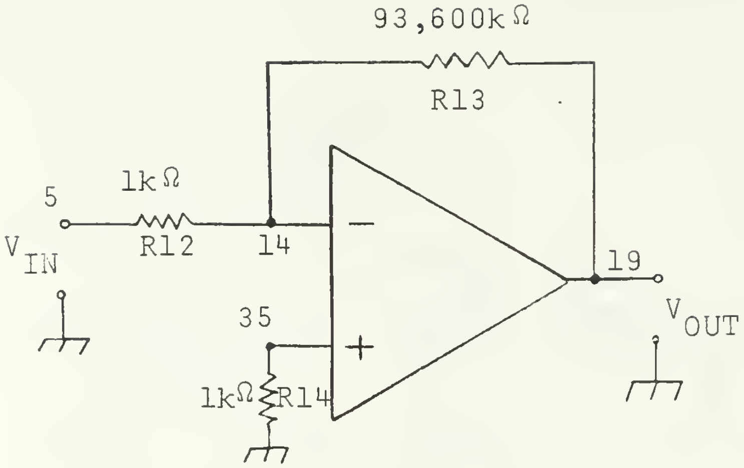


Figure 2-10 Schematic of Circuit Used for DC Analysis of Basic Model(for Transistor Collector Current Validation)

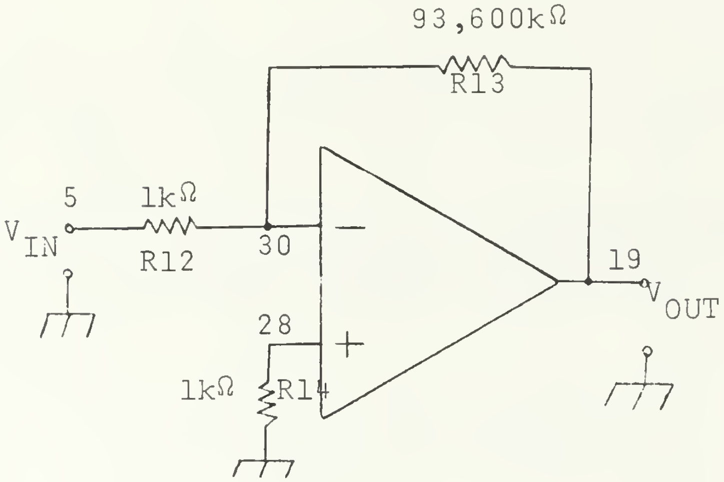


Figure 2-11 Schematic of Circuit Used for DC Analysis of Basic Model(for Offset Analysis)

5. A DC analysis was performed to determine the voltage and current offset of the model. The offset of this model was slightly better than that of a typical LM741, probably owed to the fact that matched transistors were used for the input stage transistors, something that is not usually achievable in the real world. Figure 2-2 shows the results of the offset analysis. Appendix H shows the program used to generate the results and Figure 2-11 shows the schematic of the circuit used in the analysis.

E. CONCLUSIONS

Based upon the results obtained from the analyses of the basic computer model, the model was considered to closely simulate the characteristics of the LM741 and was considered suitable for use in studying the characteristics of the Composite Operational Amplifier (CNOA). The difficulties encountered in the slew rate analysis were not considered severe enough to limit further study of the CNOA. Efforts were made to obtain a full set of SPICE parameters from various sources, however this was found to be closely held data and the efforts were to no avail. As such, most transistor parameters was allowed to default to SPICE assigned values. The combined effect of these values and the high degree of complexity of the basic model was believed to at times cause problems in analysis of circuits, specifically the DC analysis of the circuits would not converge and thus the intended analysis could proceed no further. Despite these types of problems, SPICE most generally performed adequately.

III. THE COMPOSITE OPERATIONAL AMPLIFIER

A. BACKGROUND

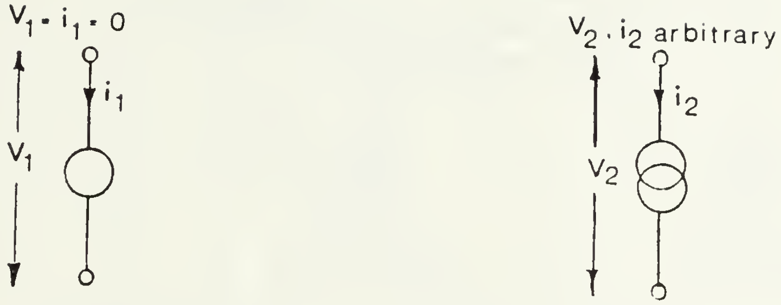
Chapter I discussed the limitations of state-of-the-art Operational Amplifiers (OAs) in terms of their bandwidth, slew rate and offset and iterated methods for improving their performance. This chapter presents the Composite Operational Amplifier (CNOA) as an alternative to overcome the limitations imposed by these methods. The concept of nullator-norator pairing to generate then CNOA is presented and the characteristics of the C2OA as a finite gain amplifier are studied through the use of computer simulation, theoretical, and experimental results. The superiority of the CNOA as an extended bandwidth (BW) amplifier with improved slew rate and offset characteristics will be shown. This research is limited to the C2OA, however the general results may be extended to the C3OA and C4OA.

B. GENERATION OF THE C2OA

The realization of the C2OA is based upon an application of the concepts of nullators, norators, and nullors. The nullator is defined as a theoretical one-port device which will neither sustain a voltage or current (i.e., $V_1=i_1=0$). The norator is defined as a theoretical one-port device which will sustain an arbitrary voltage and pass an arbitrary current which are independent of each other. A nullator and a norator may be combined into a two-port device, with the nullator as port 1 and the norator as port 2, to create a nullor [Ref. 12]. Figure 3-1 shows a schematic of an a nullator, a norator, and an OA in its nullor representation. A nullator-norator equivalent network consisting of n nullators and n norators yields n! equivalent networks [Ref. 2: p. 13]. So, for a nullator-norator network consisting of two nullators and two norators there exists two nullor equivalent networks. This is depicted in Figure 3-2. Each of the two networks shown can be arranged as in Figure 3-3 and thus a nullor equivalent network consisting of two nullors corresponds to four physical networks.

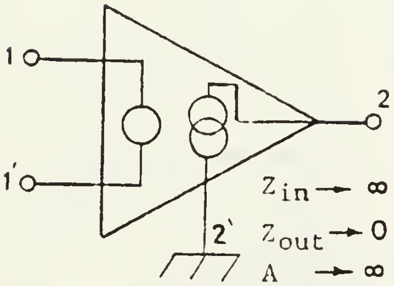
Utilizing the above concepts the C2OA may now be constructed by combining a second amplifier of gain H with a single OA. This network corresponds to a nullor. Figure 3-4 shows an example of this pairing. If possible pairings of these two amplifiers are considered, i.e., if the OA and the nullor are combined in every possible manner, there are a total of 192 networks. Of these, 136 represent actual nullors, that is, the elements of signals can assume arbitrary values. The resulting C2OAs are examined in accordance with the following criteria [Ref. 2: p. 18].

1. They must satisfy the necessary (but not sufficient) conditions for stability. This is realized if the



The Nullator

The Norator



The OA (VCVS) Nullor Representation

Figure 3-1 The Singular Elements Representations of the OA

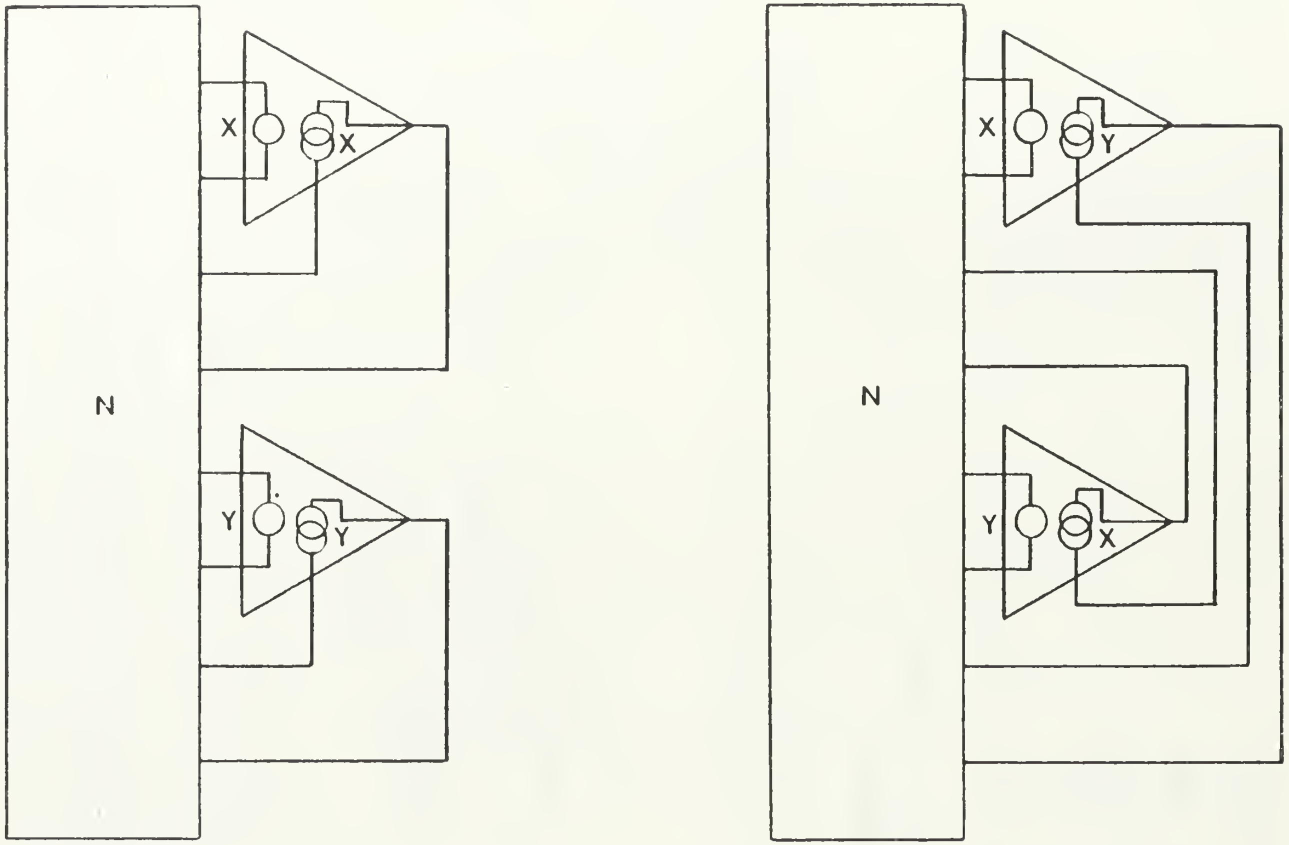
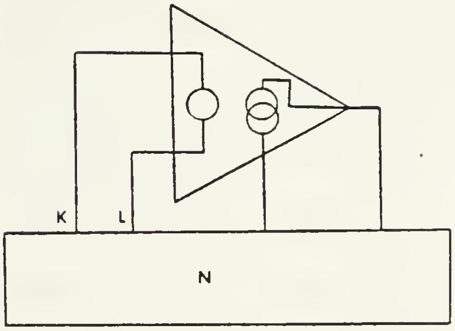
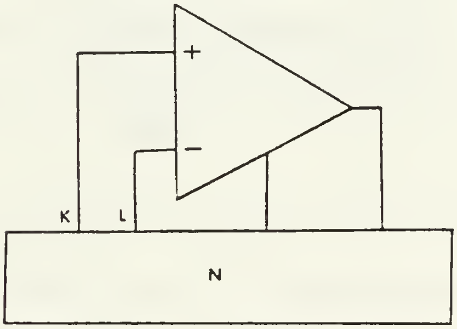
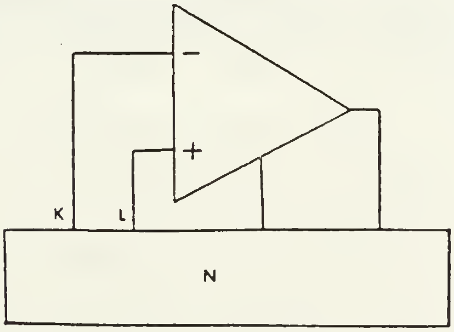


Figure 3-2 Two Alternative Nullor Equivalent Networks Obtained from a Single Nullator-Norator Network



(Circuit Containing One Nullor)





(Two Alternative Physical Circuits)

Figure 3-3 Replacement of Nullors by Physical Networks

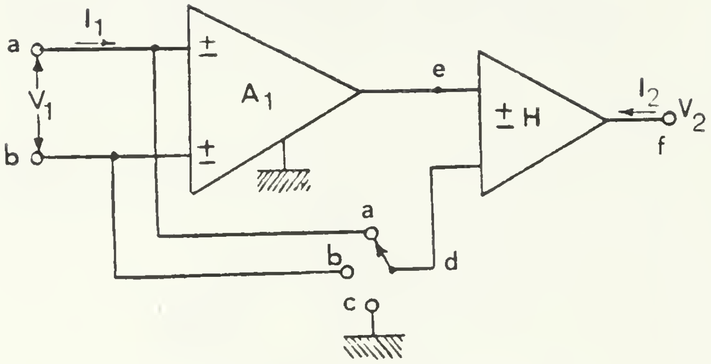


Figure 3-4 An Example Network for Generating a Composite Operational Amplifier Using Two Single OAs (C20A)

denominator of the inverting and non-inverting open loop gain equations have no change in sign.

2. They must not require single OAs with matched GBWPs and must have low sensitivity with respect to their components. This is achieved if none of the coefficients in the open loop gain equations are realized by differences.

3. No right-hand S-plane (RHS) zeroes due to a single pole should be allowed in the closed loop gain equations of the C2OA's (for minimum phase shifts).

4. The external terminal performance should be the same as that of the single OA.

5. The actual transfer function relationship should indicate an extended useful frequency operation.

6. There should be minimum gain and phase deviation from ideal.

Four of the 136 C2OAs examined for acceptable performance in accordance with the above criteria were considered satisfactory. These configurations are shown in Figure 3-5. The alpha (α) shown in that figure is the ratio of the resistors which connect the single OAs. The same basic approach shown here can be used to generate the C3OA and C4OA.

It was shown in Chapter I (equation (1)) that the expression for the dc open loop gain of a single OA is given as

$$A(\omega) = \frac{A_o}{1 + j\omega/\omega_m} \qquad (1)$$

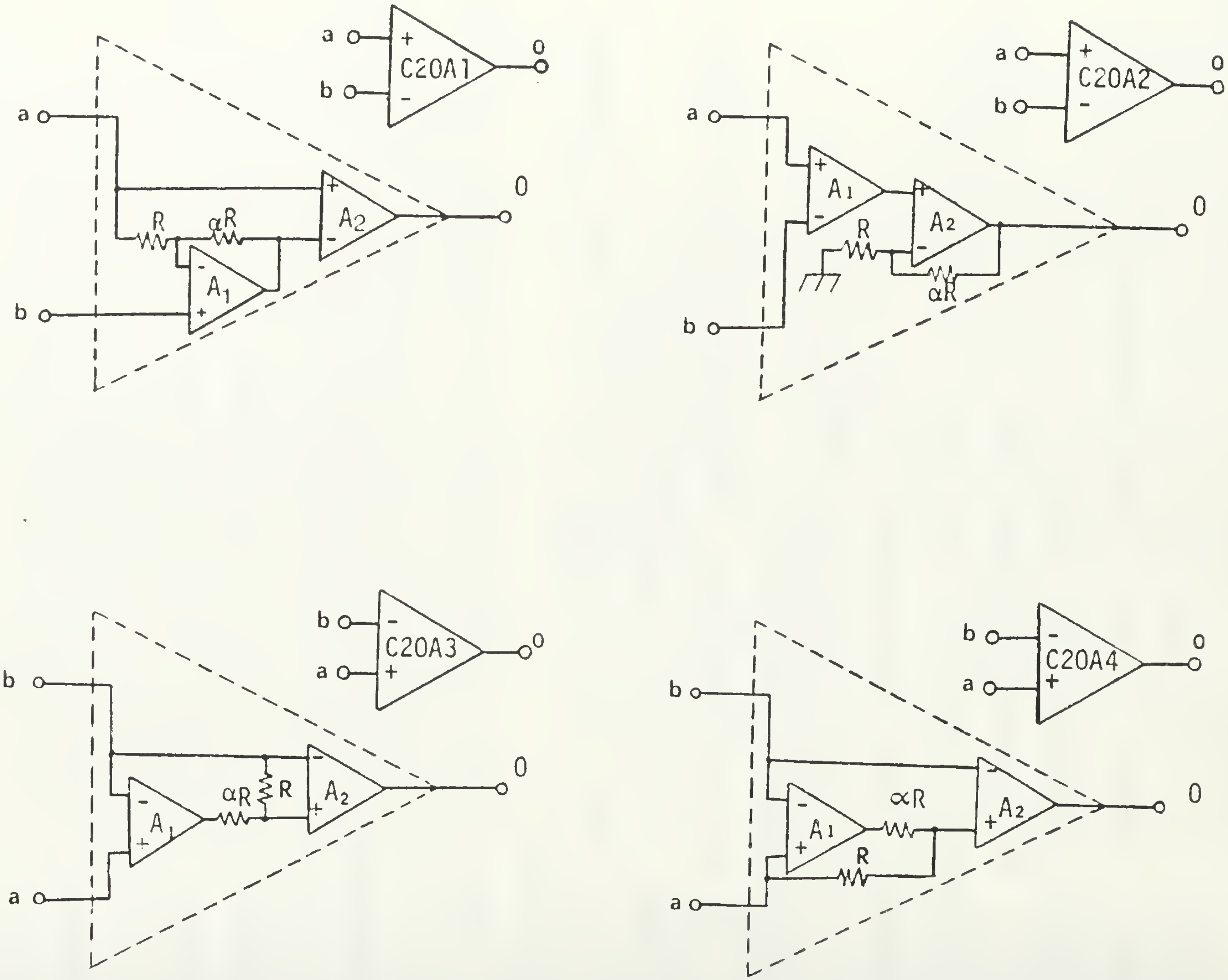


Figure 3-5 The Extended Bandwidth Composite Operational Amplifiers (C20As)

Equation (2) from Chapter I gave the GBWP of a single OA as

$$\omega_u = A_o \omega_m \tag{2}$$

From equations (1) and (2) above, the open loop gain of the single OAs utilized in constructing the C2OAs can be written as

$$A_i = \frac{A_{oi} \omega_{mi}}{\omega_{mi} + s} = \frac{\omega_{ui}}{s + \omega_{mi}} \tag{3}$$

where A_{oi}, ω_{mi}, and ω_{ui} are the DC open loop gain, the 3 dB bandwidth, and the GBWP of the ith single OA, respectively.

The input-output relationship for the C2OA has the general form $V_{ox} = V_a A_{ai}(s) - V_b A_{bi}(s)$, i=1 to 4. The development of the input-output relationship for the C2OA2 of Figure 3-6 is shown here. From the basic relationship for a single OA,

$$V_a = (V_1 - V_2) A_2 \tag{4}$$

and

$$V_1 = (V_a - V_b) A_1 \tag{5}$$

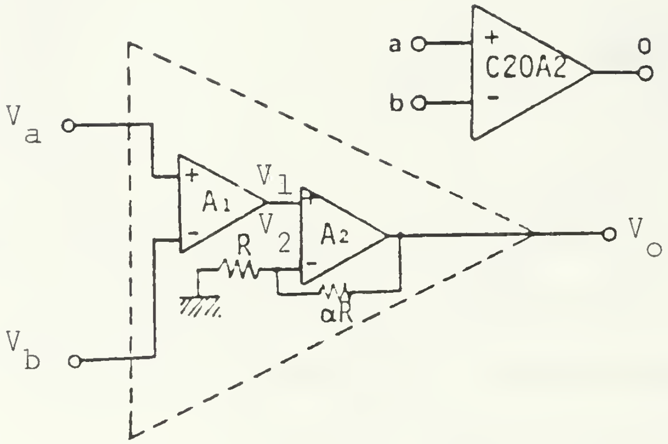


Figure 3-6 C20A2 Utilized to Derive the Open Loop Input-Output Relationship

From Eqns. (4) and (5),

$$V_o = (V_a - V_b)A_1A_2 - V_2A_2 \qquad (6)$$

Also,

$$\frac{V_o}{(1+\alpha)R} = \frac{V_2}{R}$$

which also gives,

$$V_2 = \frac{V_o}{1+\alpha} \qquad (7)$$

Substituting eqn. (7) into eqn. (6) gives,

$$V_o = (V_a - V_b)A_1A_2 - \left(\frac{V_o}{1+\alpha}\right)A_2 \qquad (8)$$

which gives the input-output relationship

$$V_o = V_a \frac{A_1A_2(1+\alpha)}{A_2+(1+\alpha)} - V_b \frac{A_1A_2(1+\alpha)}{A_2+(1+\alpha)} \qquad (9)$$

Similar analysis may be utilized to develop the input-output relationships for the other three C2OAs.

Assuming identical OAs, that is,

$$A_{01} = A_{02} = A_o \text{ and } \omega_1 = \omega_2 = \omega_x$$

and the C2OA2 in an inverting amplifier configuration with $V_a = 0$, the dc gain for the C2OA2 is given by

$$A_{OC2} = \frac{A_o(1+\alpha)}{1 + (1+\alpha)/A_o} \approx A_o(1+\alpha) \text{ for } (1+\alpha) << A_o \tag{10}$$

From (1) it can be seen that the C2OA2 has a single pole roll-off from ω_i/A_o to $\omega_i/(1+\alpha)$, where the second pole occurs. As α increases, the dc gain increases while the second pole frequency decreases. Similar analyses may be performed to derive the dc open loop gain equations for the other three C2OAs under consideration.

C. THE C2OA AS A FINITE GAIN AMPLIFIER

Finite gain amplifiers find use in a wide variety of applications including active filters, instrumentation, and oscillators. In Chapter I the concept of an ideal OA was discussed and it was shown that in practice the amplifier circuits which are realized through the use of OAs do not operate in an ideal manner, but are frequency dependent. Further limitations in the BW are imposed by the use of passive components in the active circuits, and efforts to minimize the effects of the passive components have proven to be less than acceptable. These efforts have included use of passive and active compensation, as well as actually utilizing wider BW OAs. Each of these methods and their associated problems were discussed in Chapter I. This section shows the use of the C2OA as the active element in the finite gain amplifier and its superiority to previous methods utilized to overcome the non-ideal characteristics of the OA.

Equation (5) from Chapter I shows that the BW of a finite gain amplifier shrinks by a factor of 1/k relative to its unity gain BW(ω_u). If two OAs are cascaded in a finite gain amplifier configuration with an overall gain of k, it can be shown that a BW shrinkage of $0.64/\sqrt{k}$ is experienced, assuming each amplifier has a gain of $\sqrt{k}$. This bandwidth shrinkage factor results from the following [Ref. 13]:

$$\frac{f_m^*}{f_m} = \sqrt{2^{1/n}-1}$$

where f_m^* is the total GBWP for the two identical stages, and f_m is the GBWP for a single stage. For two cascaded stages, n=2, so $f_m^* = .64\ f_m$. Since f_m for an inverting amplifier is $\approx\frac{f_u}{\text{gain}}$ (Eqn. (5), Ch. I), then, for the circuit with two cascade stages,

$$f_m^* = \frac{0.64 f_u}{\sqrt{k}}$$

Finite gain amplifiers in either a C2OA1 or C2OA2 configuration will be shown to have a BW shrinkage factor of $\frac{1}{\sqrt{k}}$ for Q=0.707 and somewhat greater than $1/\sqrt{k}$ for Q=1(k>>1). Figure 3-7 shows a comparison of the frequency response of a single OA, a cascaded pair of OAs, and a C2OA1 in a finite gain inverting amplifier configuration. The responses seen in that figure approximate the bandwidth shrinkage criteria previously given. The bandwidth extension advantage gained by using the C2OA is evidenced. An additional feature of the C2OA is that it requires only two accurate gain determining components vice four for the cascade realization. The computer programs used to generate the results in Figure 3-7 are contained in Appendices B, I, and J, and the schematics of the circuits utilized to produce those results are shown in Figure 3-8.

Figure 3-9 shows the input-output relationships for the four C2OA configurations. For illustrative purposes, the derivation for the relationship given for the C2OA1 is shown here. Figure 3-10 shows the circuit under consideration.

The basic input-output relationship for the A2 OA is given as

$$V_o = -A_2 V_3$$

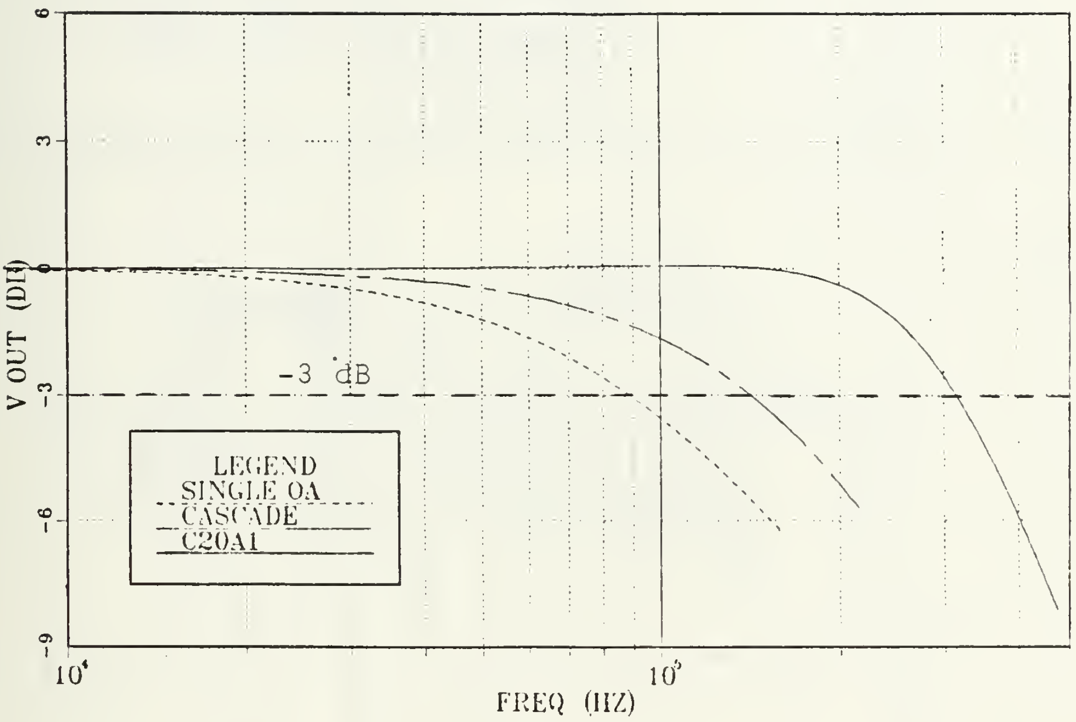


Figure 3-7 Computer Results Frequency Response of Single OA vs. Two Stage Cascade vs. C20A1 Inverting Amplifiers (K= -10)

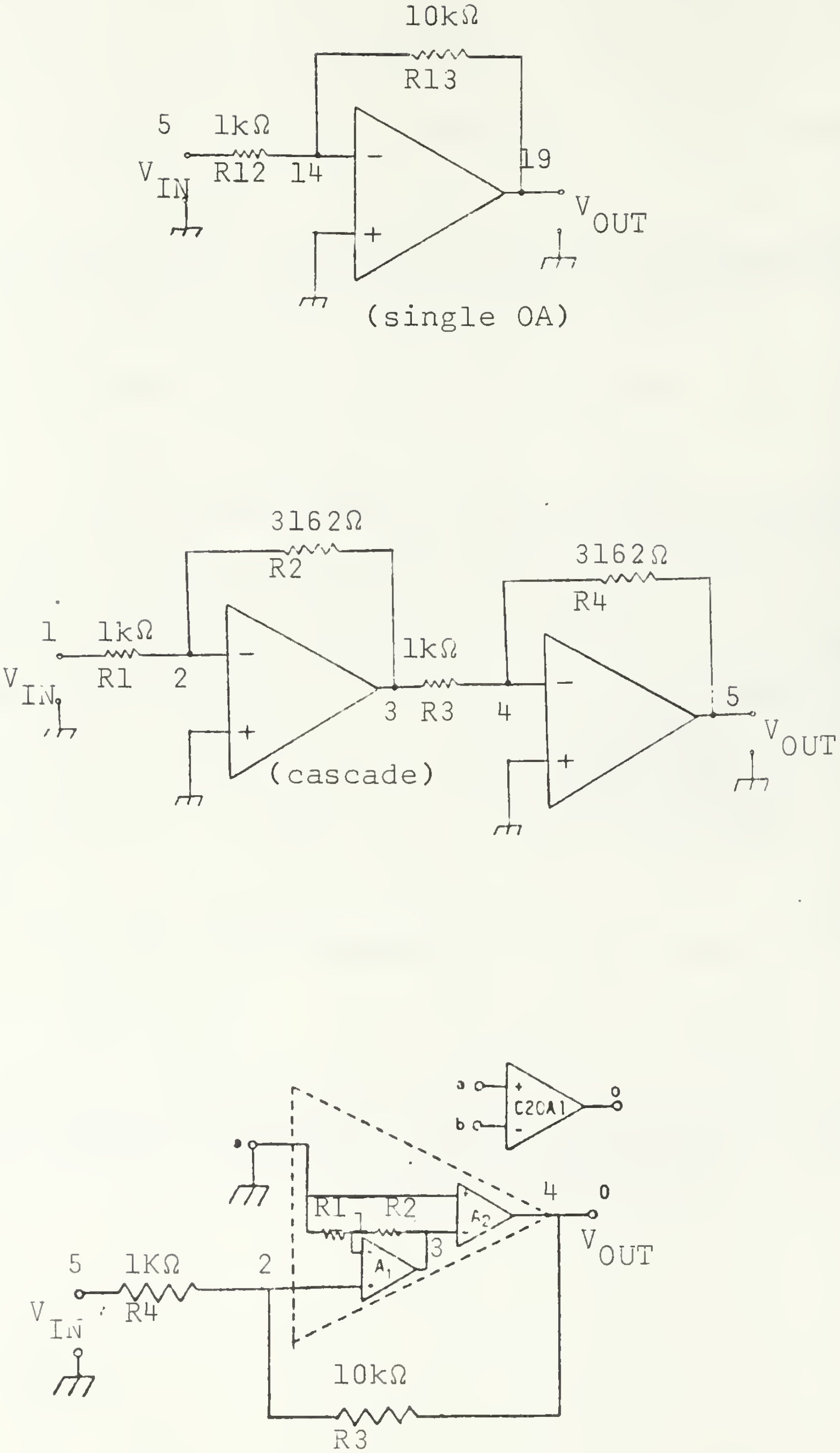
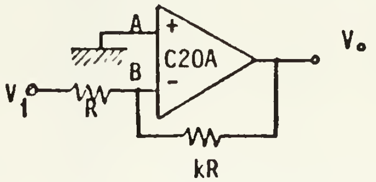
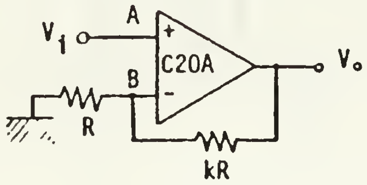


Figure 3-8 Schematic Diagram of Circuit Used to Generate the Results of Figure 3-7

C20A	Negative Finite Gain Trans. Function (Ta)	Positive Finite Gain Trans. Function (Ta)	ω_p	Q_p
C20A-1	$T_1 \dfrac{1}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$T_1 \dfrac{(1+S/\omega_1)}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$\sqrt{\dfrac{\omega_1\omega_2}{1+k}}$	$\dfrac{(1+\alpha)}{\sqrt{1+k}} \sqrt{\dfrac{\omega_2}{\omega_1}}$
C20A-2	$T_1 \dfrac{1}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$T_1 \dfrac{1}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$\sqrt{\dfrac{\omega_1\omega_2}{1+k}}$	$\dfrac{(1+\alpha)}{\sqrt{1+k}} \sqrt{\dfrac{\omega_1}{\omega_2}}$
* C20A-3	$T_1 \dfrac{(1+S/\omega_1)}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$T_1 \dfrac{1}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$\sqrt{\dfrac{\omega_1\omega_2}{(1+k)(1+\alpha)}}$	$\sqrt{\dfrac{(1+k)(1+\alpha).\omega_1}{\omega_2}}$
C20A-4	$T_1 \dfrac{[1+(1+\alpha)S/\omega_1]}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$T_1 \dfrac{(1+\alpha S/\omega_1)}{1 + (S/\omega_p Q_p) + (S^2/\omega_p^2)}$	$\sqrt{\dfrac{\omega_1\omega_2}{(1+k)(1+\alpha)}}$	$\sqrt{\dfrac{(1+k)}{(1+\alpha)} \cdot \dfrac{\omega_1}{\omega_2}}$
				
	$\dfrac{V_o}{V_1} = -k = T_1$	$\dfrac{V_o}{V_1} = (1+k) = T_1$	T_1(ideal Transfer Function)	

* $\alpha R_1 \ll kR$ (for maximum ω_p)

Figure 3-9 Input-Output Relationships for the C20As

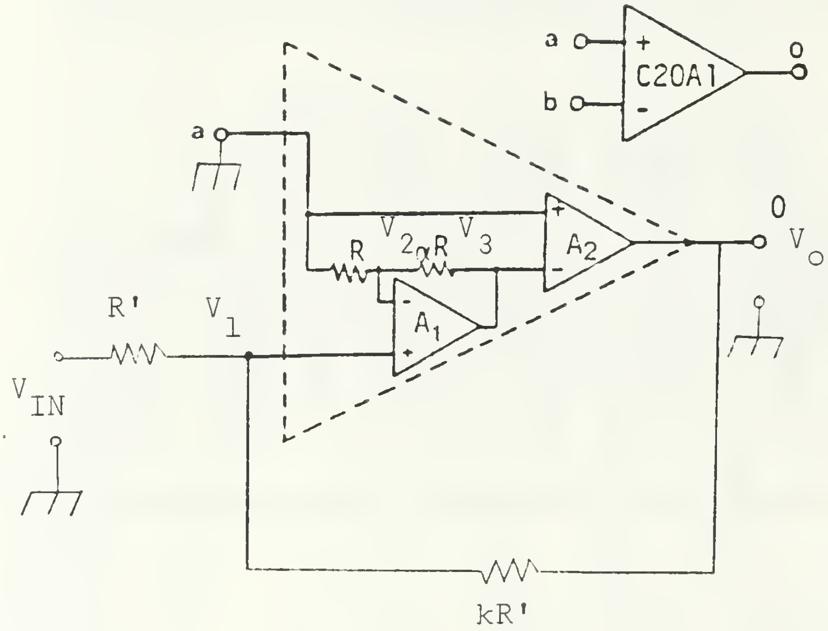


Figure 3-10 C20A1 Schematic Used to Derive Input-Output Relationship

which yields

$$V_3 = \frac{-V_o}{A_2} \tag{11}$$

Also,

$$\frac{V_3-0}{(1+\alpha)R} = \frac{V_2-0}{R}$$

which gives,

$$V_3 = V_2(1+\alpha) \tag{12}$$

From Eqns. (11) and (12)

$$V_2 = \frac{-V_o}{A_2(1-\alpha)} \tag{13}$$

By definition,

$$A_1(V_1-V_2) = V_3$$

So from eqns. (13) and (11),

$$\frac{-V_o}{A_1A_2} = V_1 + \frac{V_o}{A_2(1+\alpha)}$$

which gives,

$$V_1 = -V_o \frac{(1+\alpha)+A_1}{A_1A_2(1+\alpha)} \tag{14}$$

Now considering the currents for the external loop,

$$\frac{V_o-V_{IN}}{(1+k)R'} = \frac{V_1-V_{IN}}{R'}$$

which gives,

$$\frac{V_o+kV_{IN}}{(1+k)} = V_1$$

but from (14),

$$\frac{V_o+kV_{IN}}{(1+k)} = -V_o \frac{(1+\alpha)+A_1}{A_1A_2(1+\alpha)}$$

Using $A_{oi} \simeq \frac{\omega_{mi}}{s}$ (from eqn. (3)), it can be easily shown that

$$\frac{V_o}{V_{IN}} = \frac{-k}{1 + \frac{(1+k)}{(1+\alpha)} \frac{s}{\omega_{m2}} + (1+k) \frac{s^2}{\omega_{m1}\omega_{m2}}} \tag{15}$$

The general input-output relationship for this second order circuit may be given as,

$$\frac{V_o}{V_{IN}} = \frac{-k}{1 + s/Q_p\omega_p + s^2/\omega_p^2} \tag{16}$$

Then for (15) and (16) to be equivalent for the C20A1 the following relationships must hold:

$$\omega_p = \sqrt{\frac{\omega_{m1}\omega_{m2}}{(1+k)}}$$

$$Q_p = \frac{(1+\alpha)}{\sqrt{1+k}} \sqrt{\frac{\omega_{m1}}{\omega_{m2}}}$$

The above two relationships of the four C20A configurations are shown in Figure 3-9.

Each of the transfer functions shown in Figure 3-9 has the form

$$H_a = H_i \cdot \frac{N}{D} \tag{17}$$

where H_i is the ideal transfer function realized assuming ideal OAs and

$$N = 1 + as = 1 + \frac{s}{\omega_z}$$

and

$$D = a + b_1 s + b_2 s^2 = 1 + (s/\omega_p Q_p) + s^2/\omega_p^2$$

From the above it can be seen that N/D determined the amplitude and phase deviation of H_a from H_i and b_1 and b_2 determine the stability of H_a. Also ω_z, ω_p, and Q_p are seen to be functions of the circuit parameters ω_1, ω_2, and α. Low sensitivity of H_a, ω_z, ω_p, and Q_p to the circuit parameters is guaranteed since in all of the transfer functions neither the a nor the b coefficients are realized through differences. Assuming a single pole model, the fact that the b coefficients are always positive guarantees the stability of the transfer function. It is observed from Figure 3-9 that for the C20A1, a 5% mismatch in GBWPs of the single OAs results in a change in ω_p and Q_p of no greater than 2.5%.

The necessary and sufficient conditions for the stability of the C20A1 through C20A4, when considering a two-pole OA model, can be shown to be the following [Ref. 2: p. 37]:

C20A1
& $(1+\alpha)<(1+k)/2$
C20A2

C20A3 $(1+\alpha)<\sqrt{1+k}$

C20A4 $(1+\alpha)<4\sqrt{1+k}$

From equation (17), it is desirable to choose α such that ω_p and Q_p result in an acceptable amplitude and phase deviation in H_a from H_i, while at the same time satisfying the stability conditions given above. Figure 3-11 shows the values of α required to give a $Q_p = 0.707$ (maximally flat) and $Q_p = 1$. Applying the results of the necessary and sufficient stability considerations to each of the C20As shows that the optimum configurations from both the stability and BW standpoint are the C20A1 and C20A2 designs.

D. SIMULATION RESULTS FOR THE C20A FINITE GAIN AMPLIFIER

The previous section showed theoretical relationships associated with the use of the C20A as a finite gain amplifier. Figures 3-12 and 3-15 show computer simulation results for the frequency response of the C20A used as a finite gain inverting amplifier (k= -10). Figure 3-16 shows

$C20A_i$	$1+\alpha$	Q_p	ω_p	Stability Condition for α used
C20A-1	$\sqrt{1+k}$	1	$\frac{\omega_i}{\sqrt{1+k}}$ (independent of α)	Satisfied
&				
C20A-2	$\sqrt{\frac{1+k}{2}}$	$\frac{1}{\sqrt{2}}$		Satisfied
C20A-3	0	$Q_{p_{min}} = \sqrt{1+k}$	$\frac{\omega_i}{\sqrt{1+k}}$	Unsatisfied
C20A-4	$(1+k)$	1	$\frac{\omega_i}{1+k}$	Unsatisfied
	$2(1+k)$	$\frac{1}{\sqrt{2}}$	$\frac{\omega_i}{\sqrt{2}(1+k)}$	Unsatisfied

Figure 3-11 Values of α for Maximally Flat & $Q_p=1$, with their Corresponding Bandwidth and Stability Conditions for C20As in Finite Gain Applications

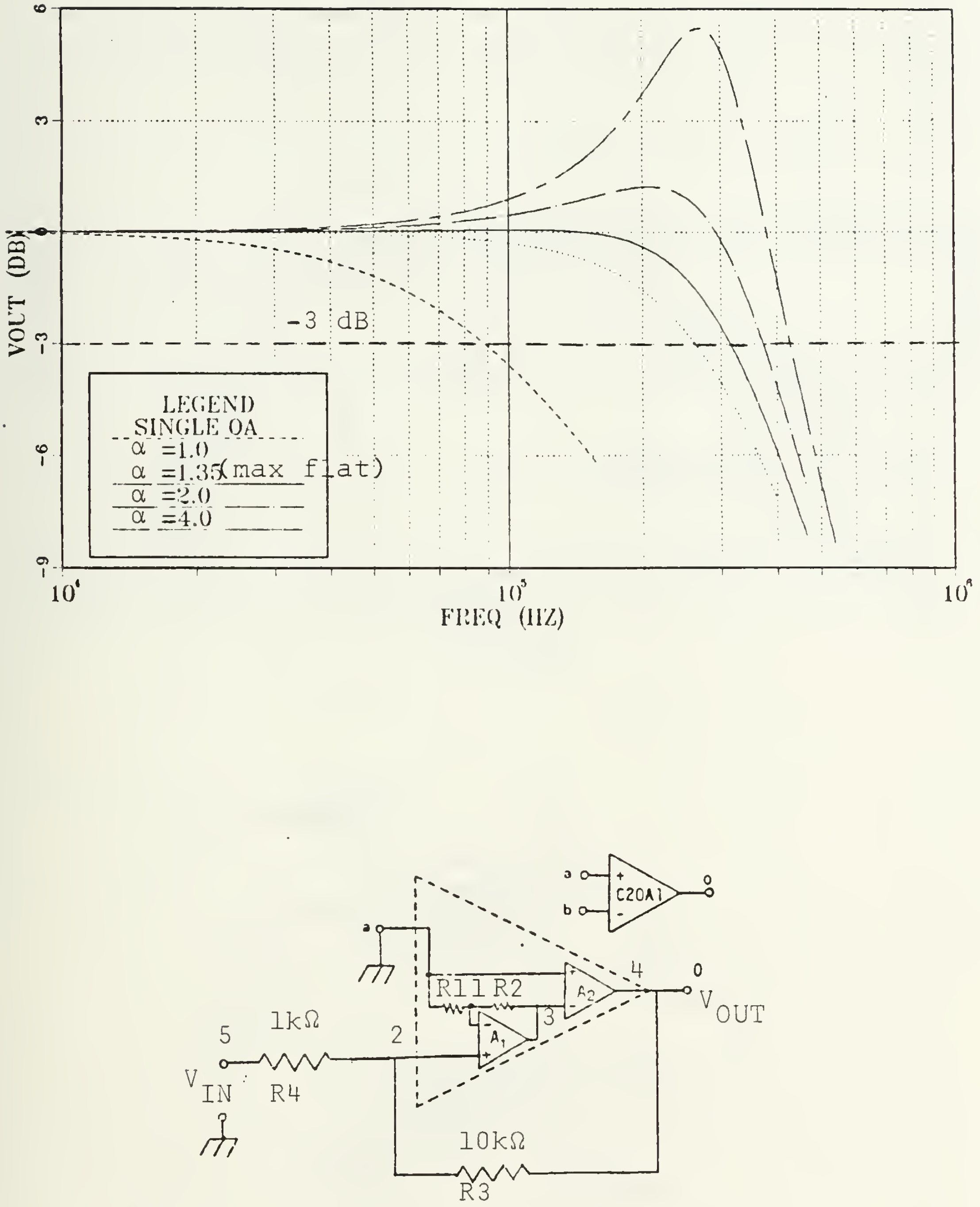


Figure 3-12 Frequency Response for C20A1 Inverting Amplifier and Circuit Schematic (k= -10)

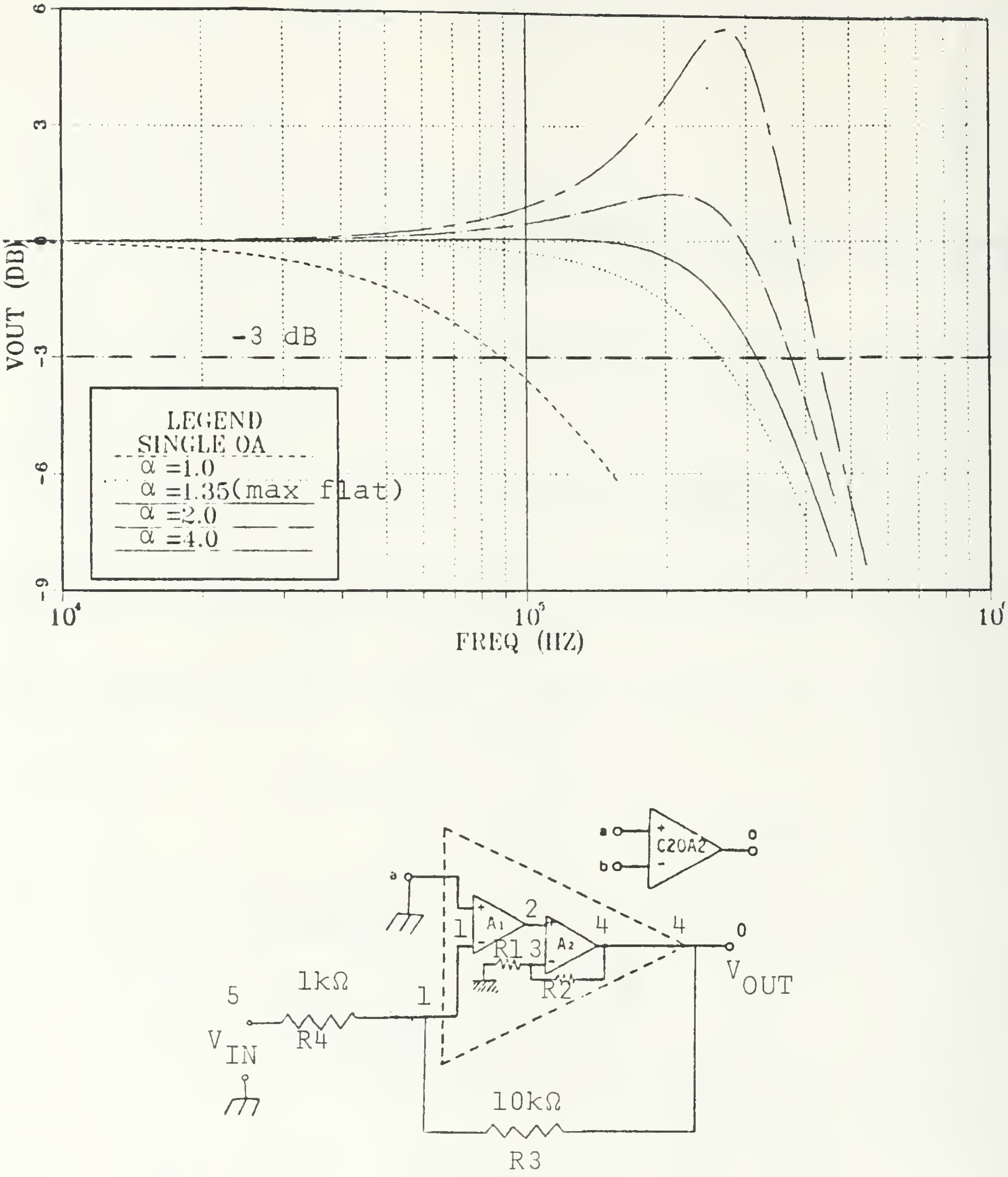


Figure 3-13 Frequency Response for C20A2 Inverting Amplifier and Circuit Schematic (k= -10)

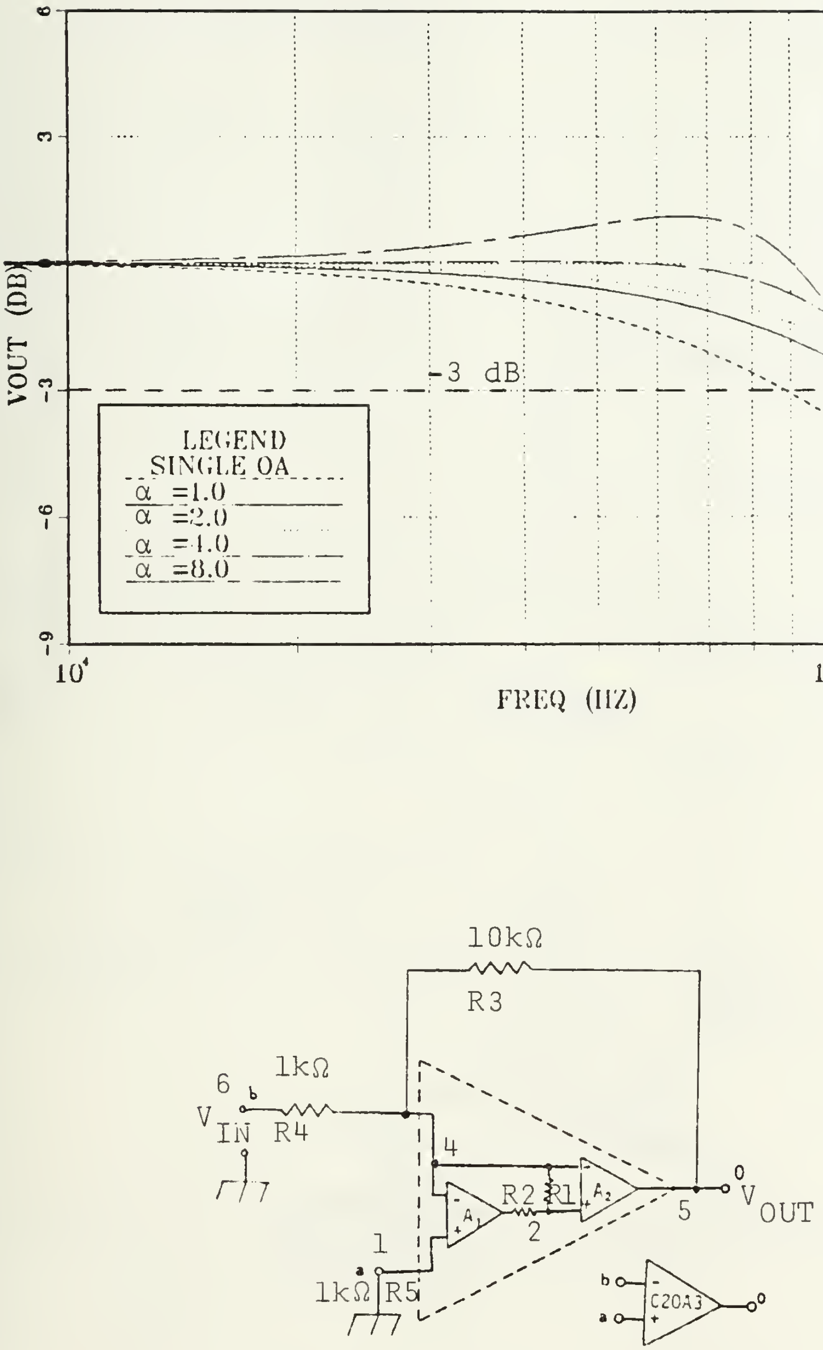


Figure 3-14 Frequency Response for C20A3 Inverting Amplifier and Circuit Schematic (k= -10)

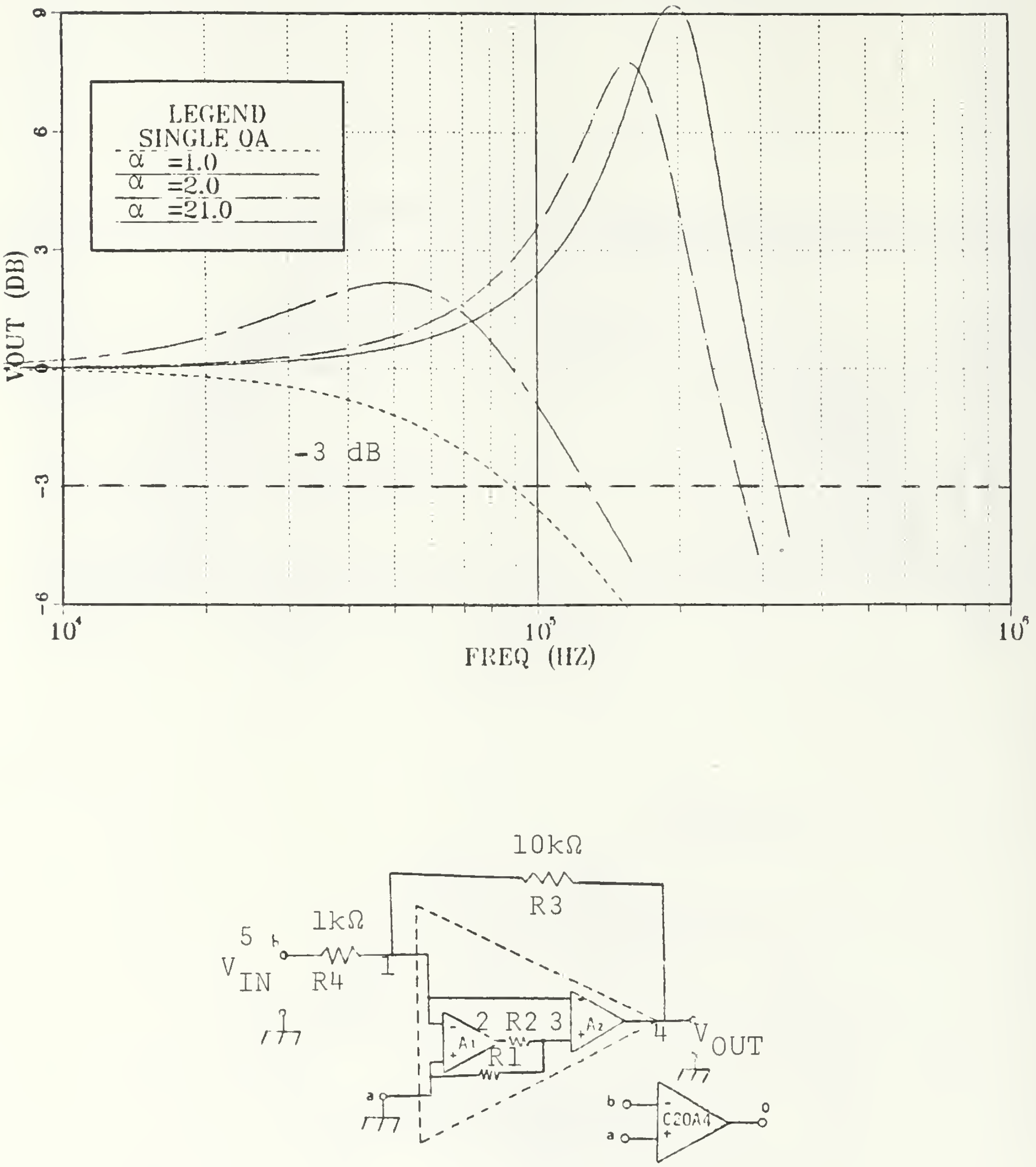


Figure 3-15 Frequency Response for C20A4 Inverting Amplifier and Circuit Schematic (k= -10)

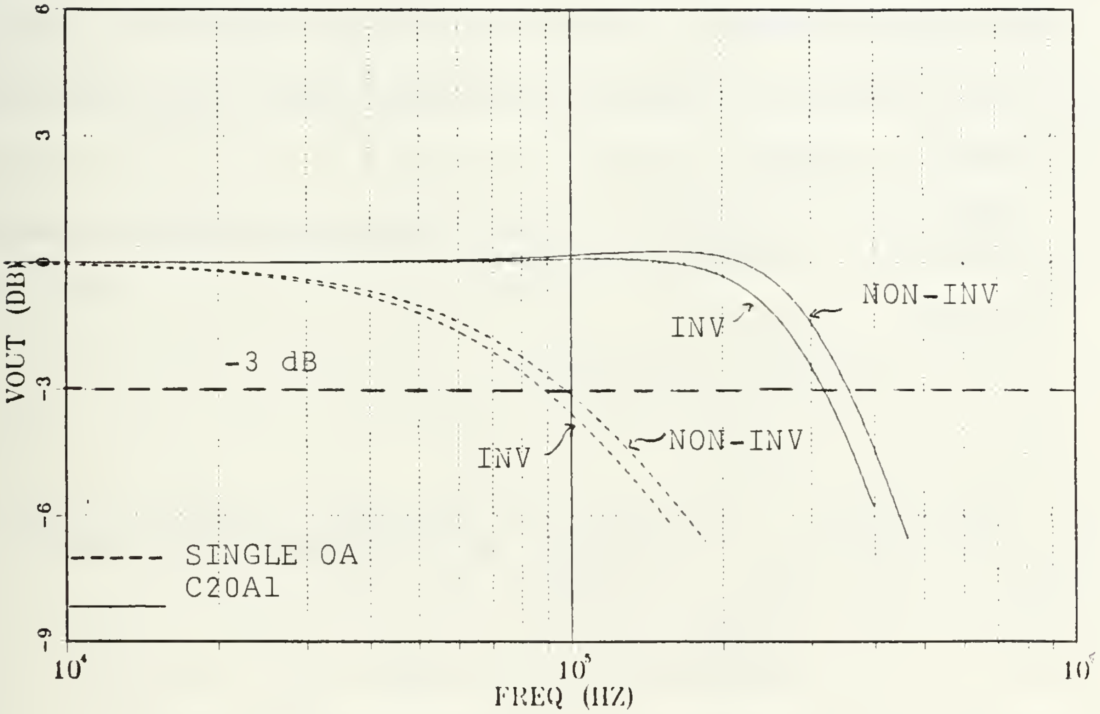


Figure 3-16 Comparison of Frequency Response for C2OA1 and Single OA in Inverting and Non-Inverting Configurations (k= 10)

the differences between the frequency response of the C20A in the inverting and non-inverting configurations. These differences are caused by the introduction of a zero in the non-inverting configuration. The transfer function of Figure 3-9 for the C20A1 shows this fact. The programs contained in Appendices J through M were used to produce Figures 3-12 through 3-16.

The results shown in Figure 3-12 are analyzed below to show the comparison with the theoretical results obtained in the previous section:

1. The output amplitude at low frequencies corresponds to that given by a single OA, i.e.,

$$\begin{aligned} V_{OUT}(\mathrm{dB}) &= 20\log(kV_{IN}) \\ &= 20\log[(10)(0.1)] \\ &= 0\ \mathrm{dB} \end{aligned}$$

2. The value of α required for maximum flatness is seen to be 1.35. This corresponds to the theoretical value given by the formula of Figure 3.9, i.e.,

$$Q_p = 0.707 = \frac{(1+\alpha)}{\sqrt{1+10}}\sqrt{\frac{\omega_2}{\omega_1}} \quad (\omega_2 = \omega_1)$$

which gives $\alpha=1.35$.

3. The ω_p for $Q_p=1.0$ corresponds to the theoretical value given by the equation of Figure 3-11, i.e.,

$$\omega_p = \sqrt{\frac{\omega_1\omega_2}{(1+k)}} = \frac{\omega_i}{\sqrt{1+k}} = 1.705\ \mathrm{MHz}$$

which gives $f_p = 2.71 \times 10^5$.

4. By using α=1.35 (max flat), an additional BW extension is observed, i.e., $f_p=3.15 \times 10^5$, which is 3.5X greater than that of a single OA.

The results for the other C2OAs may be analyzed as above and are shown to correspond to the theoretical results of the previous section. Based on the frequency response for the C2OA3 and C2OA4, together with the stability considerations given in the previous section, these two configurations seem to have limited application as finite gain amplifiers. The C2OA3 has been shown to perform well as an inverting integrator [Ref. 2: p. 62]. Chapter IV of this paper will show the use of the C2OA3 and C2OA4 in active -RC filters.

The C2OA 1 was further utilized to demonstrate the low sensitivity and high degree of stability of the composite configuration. Figure 3-17 shows the effect on bandwidth by varying the gain of both the C2OA 1 and the single OA. It is observed that for both of these amplifiers as k increase, BW decreases. The bandwidth shrinkage, however, is seen to be much greater for the single OA. Figure 3-18 shows the effect of varying power supply voltage on the C2OA1 and the single OA. It can be observed that for decreased power supply voltages, the C2OA1 continues to perform better than the single OA. Finally, the good stability of the C2OA1 can be observed from the results of Figure 3-19, where the resistor-ratio was varied by ±5% and the effects on circuit operation are observed. From these computer

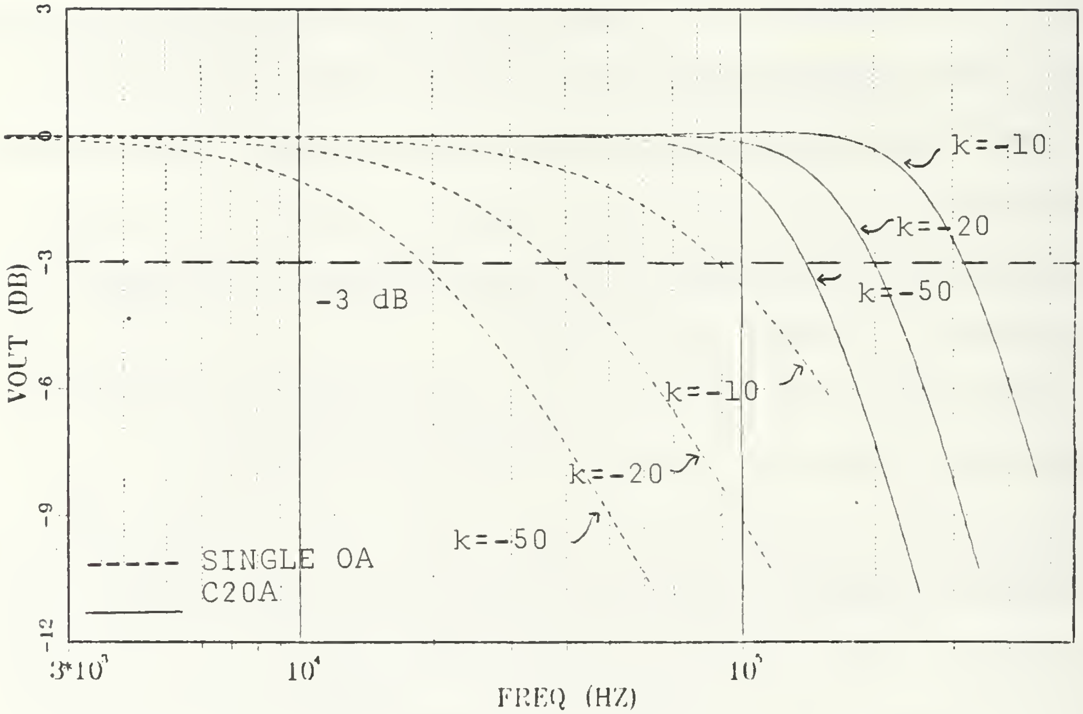


Figure 3-17 Effect of Varying Gain for Single OA vs. C20A1 Inverting Amplifiers (k= -10, -20, -50)

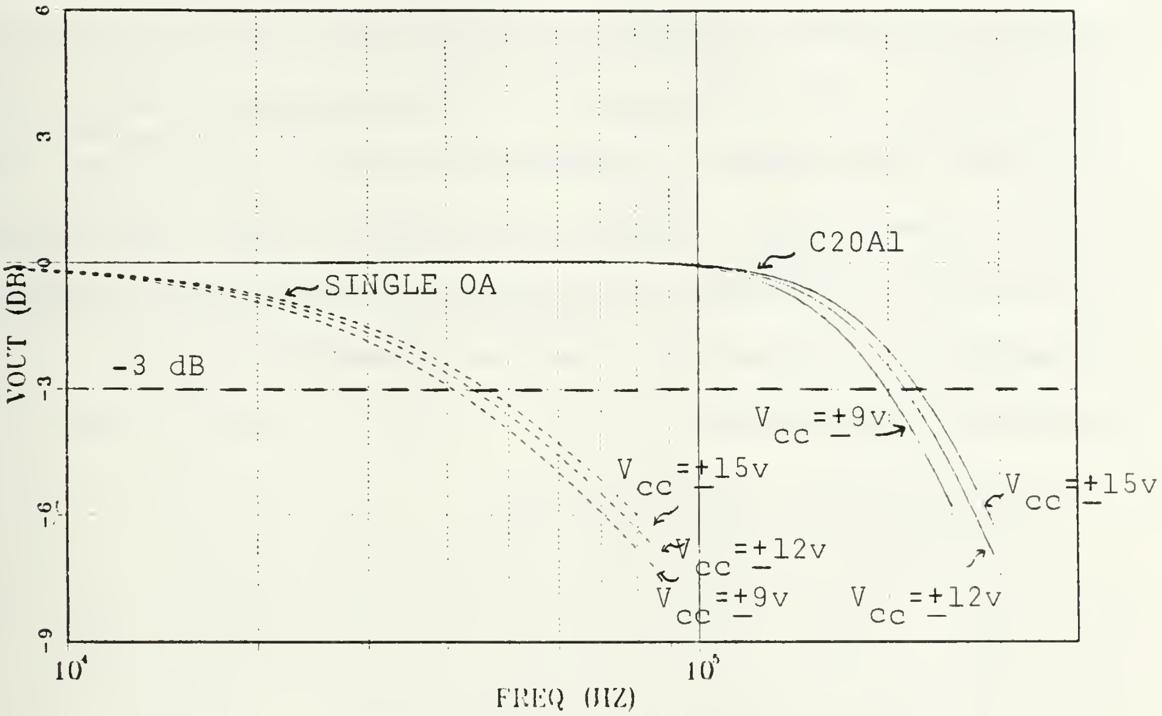


Figure 3-18 Effect of Varying Power Supply Voltage for Single vs. C20A1 Inverting Amplifier (k= -20)

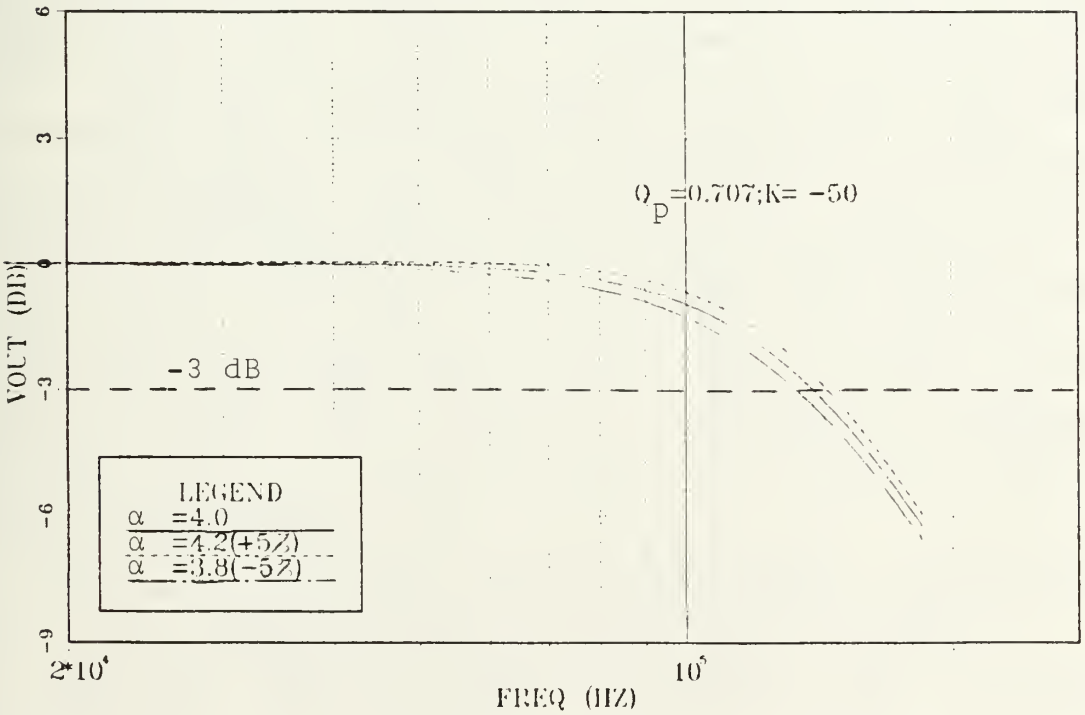


Figure 3-19 Effect of Resistor-Ratio (α) Variation by ±5%

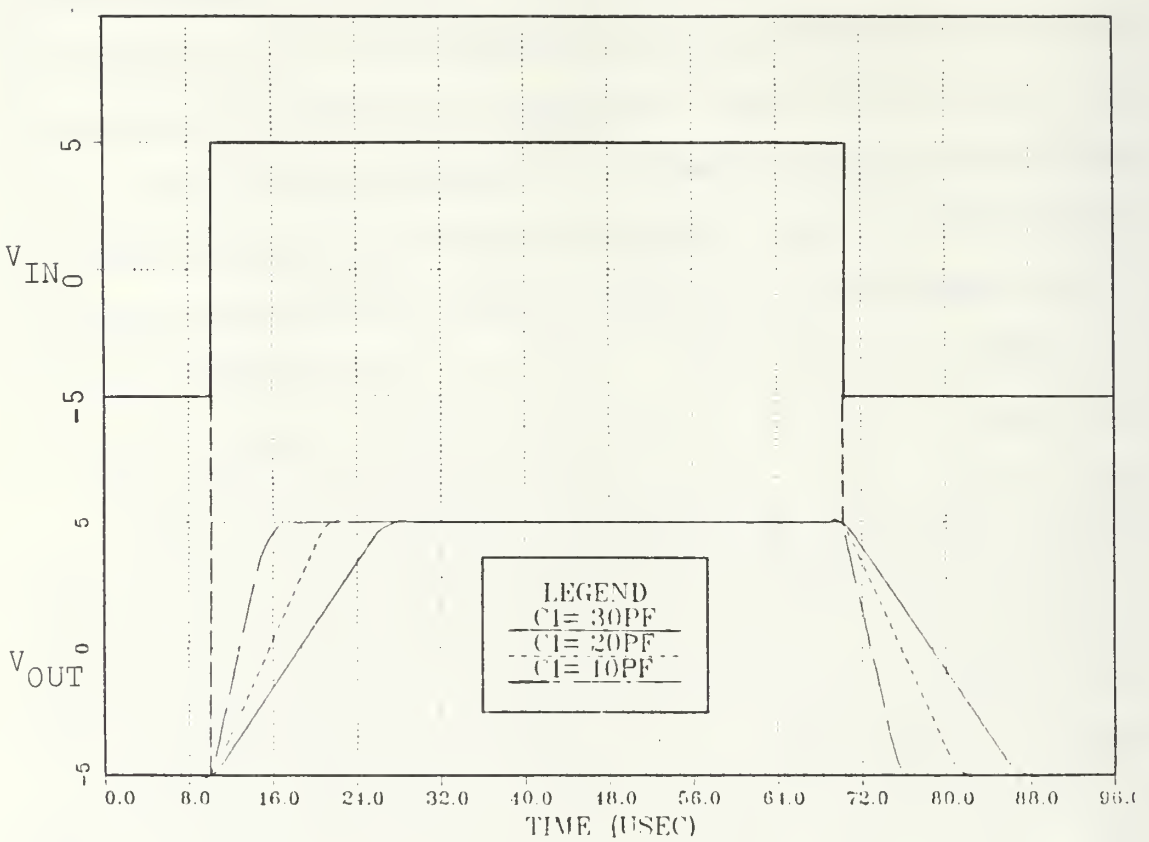
simulation results it can be seen that a significant BW extension over the single OA is attained by the of a C2OA. Additionally, the C2OA performs at least as well as the single OA with respect to sensivity to circuit element values, power supply variations, stability, and versatility. The results discussed in this paragraph can be duplicated by modification of the appropriate parameters in the program of Appendix L.

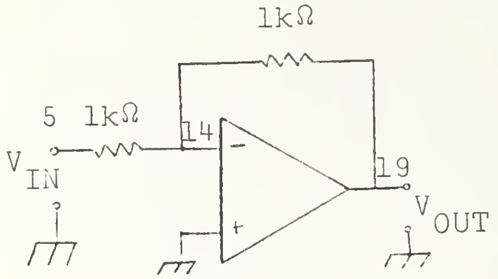
E. SLEW RATE AND OFFSET ANALYSES

Chapter I discussed the methods which have been utilized to improve the slew rate (SR) of the single OA, as well as the limitations inherent to these methods. In each of the methods presented, an increase in SR of the OA resulted in an increase in offset voltage. This section will show how the C2OA can be employed to overcome this effect. The analyses of this section combine computer simulation, theoretical, and experimental results. The slew rate analysis of the C2OA will show that its slew rate is determined by the slew rate of the output OA (A2) and the offset analysis of the C2OA will show that its offset is determined by the offset of input OA (A1). Finally, it will be shown how these two features can be combined to produce a high speed, high accuracy Operational Amplifier.

To simulate the performance of OAs to prove the assertion above required the design of single OAs with different slew rates. This was accomplished by varying the value of the compensating capacitor in the basic LM741 model. The computer program of Appendix E with C1=10pf, 20pf, and 30pf was used to simulate the different slew rates. The computer simulation results of this effort are shown in Figure 3-20. It can be seen that the slew rate of the single OA may be enhanced by decreasing the value of the compensating capacitor. The OAs #1 and #3 were selected to be used in the C2OA. The four possible combinations of these two OAs were considered in the C2OA 1 inverting amplifier configuration and the simulation results are shown in Figure 3-21. It can be seen from these results that the output OA(A2) is the OA which controls the slew rate of the composite configuration. It is noted that when a slow OA and a faster OA are combined, with the faster OA as A1, that an overshoot exists. Figure 3-22 shows that the amplitude of this overshoot can be adjusted by adjusting α. The program of Appendix N was utilized to obtain these results. This slew rate analysis was then repeated experimentally and the results are shown in Figure 3-23. From both the computer and experimental results it can be seen that the slew rate of the C2OA is controlled by the output OA (A2) of the configuration.

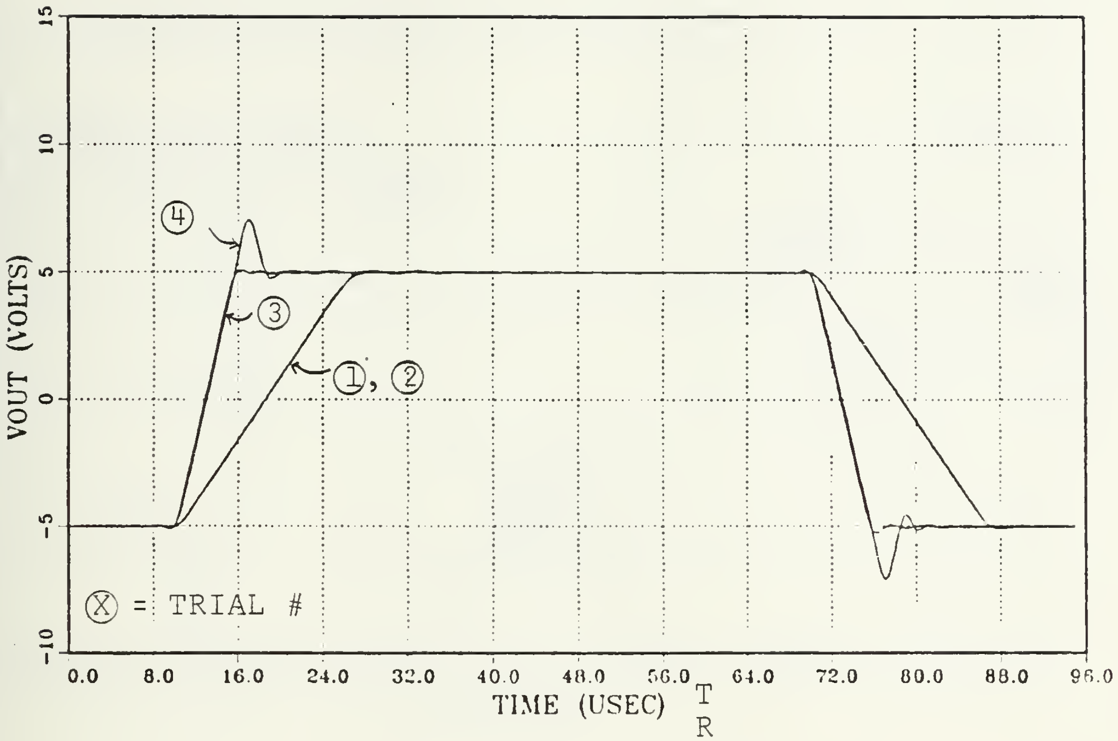
The above results can also be easily proven by applying the results obtained in Chapter I for the full-power



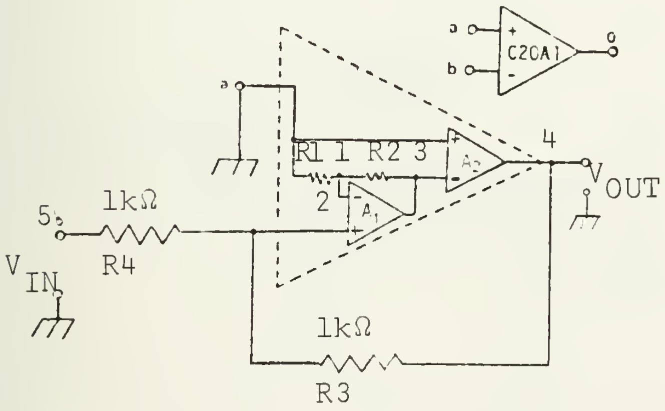


OA	C1	+SR (V/μsec)	-SR (V/μsec)
#1	30pF	0.615	0.615
#2	20pF	0.926	0.903
#3	10pF	1.86	1.79

Figure 3-20 Computer Model Slew Rate Results for Single OA



TRIAL	A1	A2	+SR (V/µsec)	-SR (V/µsec)
①	1	1	0.615	0.615
②	1	3	1.86	1.85
③	3	3	1.86	1.85
④	3	1	0.615	0.615



Note:

OA #1=+0.615, -0.615 v/µsec

OA #3=+1.86, -1.79 v/µsec

Figure 3-21 Computer Model Slew Rate Results for C20A1

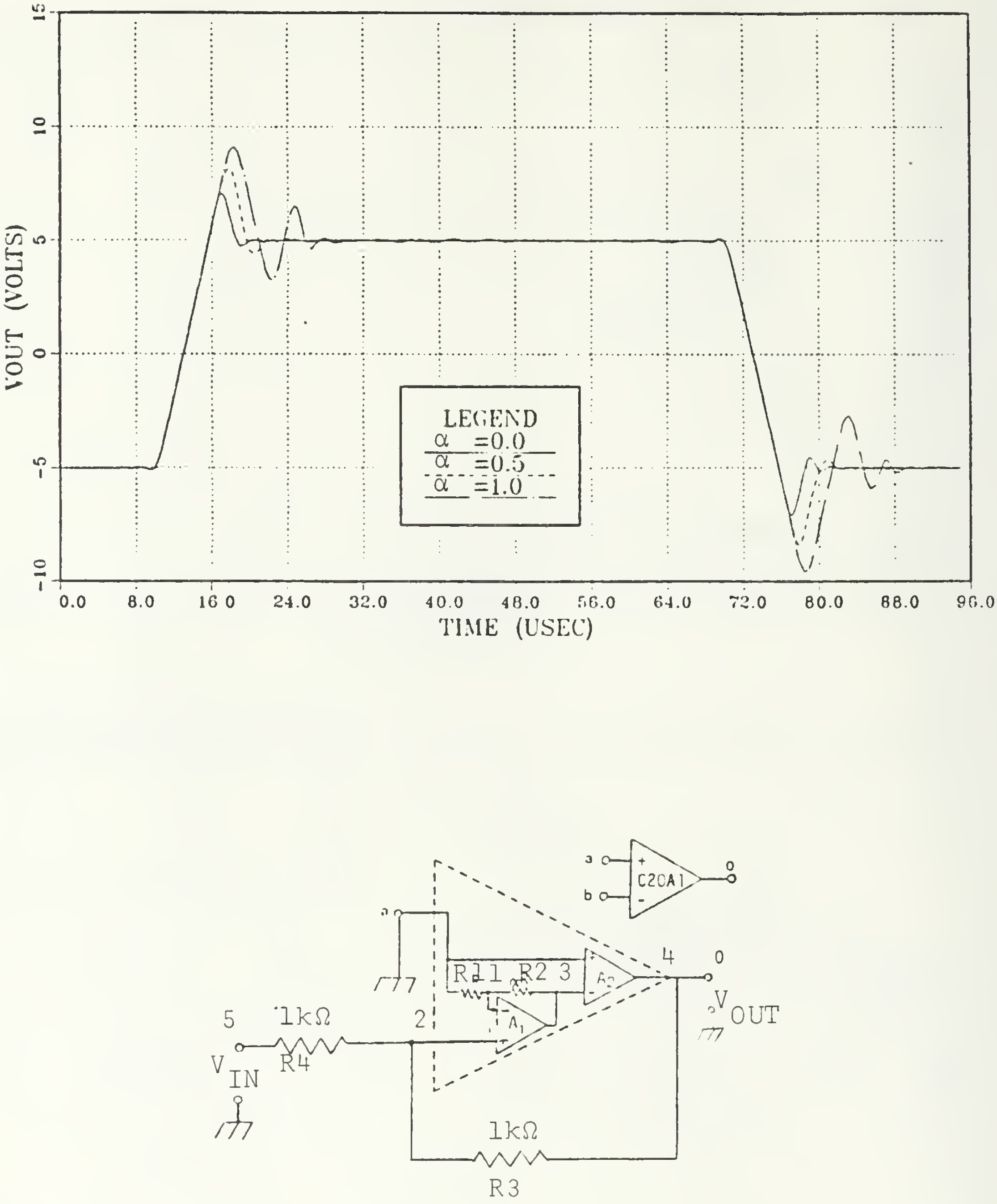
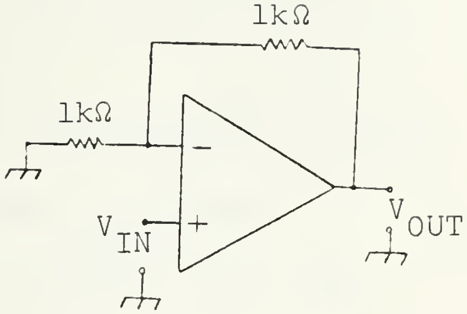


Figure 3-22 Effects of Varying α on Slew Rate Overshoot of C20A1

SINGLE OA ANALYSIS

OA#	SLEW RATE (v/µsec)
1	± 0.88
2	± 0.91
3	± 0.67
4	± 0.67



C20A1 ANALYSIS

A1	A2	SLEW RATE (v/µsec)
1	3	± 0.625
3	1	± 0.87
2	1	± 0.86
4	3	± 0.67

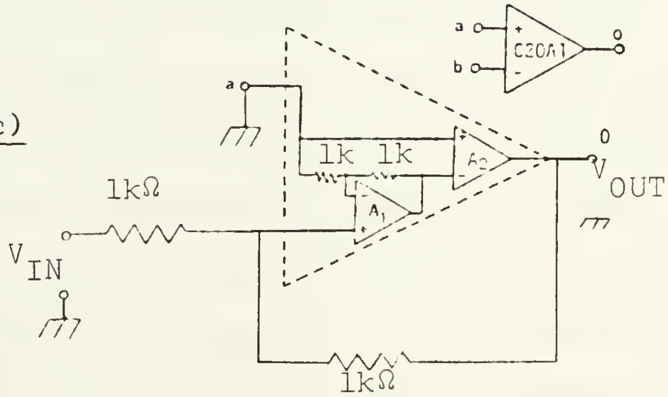


Figure 3-23 Experimental Results of C20A1 Slew Rate Analysis

bandwidth (ω_{max}). From equation (9) of Chapter I

$$SR = \left.\frac{dV_o}{dt}\right|_{max} = \omega V_p \qquad (18)$$

and from equation (10) of Chapter I

$$\omega_{max} = \frac{1}{V_p} \left.\frac{dV_o}{dt}\right|_{max} \qquad (19)$$

Combining eqns. (18) and (19) above gives

$$\omega_{max} = \frac{1}{V_p} \times SR \qquad (20)$$

The result of equation (20) can be applied to the C20A1 of Figure 3-22 and an interesting conclusion is found. First assume that the slew rates of A1 and A2 are equal. Since it can be easily shown that the voltage at the output of A2 is much larger than that at the output of A1, it is clearly seen that the maximum frequency according to eqn. (20) will be determined by A2. Then by using a high slew rate OA in place of A2 will allow the C20A to work at a much higher frequency, with very little effect due to the dlew rate of A1. The result will be a high slew rate C20A with speed as fast as the speed of A2. This result agrees with the simulation and experimental results achieved earlier.

Figure 3-24 shows the theoretical offset relationships for the C20A. From these relationships it can be seen that the offset voltage of the C20A is determined primarily by the offset voltage of the A1 amplifier. For purposes of illustration, the derivation of the relationship for the C20A4 is shown below. Figure 3-25 shows a schematic of the circuit under consideration.

Since,

$$\frac{V_1-V_2}{\alpha R} = \frac{V_2-V_3}{R}$$

then,

$$V_1+\alpha V_3 = (1+\alpha)V_2 \qquad (21)$$

Also,

$$V_1 = A_1V_3 \qquad (22)$$

Substituting eqn. (21) into (22) gives

$$A_1V_3+\alpha V_3 = (1+\alpha)V_2$$

which simplifies to

$$V_3 = V_2 \frac{(1+\alpha)}{(A+\alpha)}$$

C20A-1	$V_{off} \cong V_{off1} + (V_{off2}/\alpha)$
C20A-2	$V_{off} = V_{off1} + (V_{off2}/A_1)$
C20A-3	$V_{off} = V_{off1} + [V_{off2}(1 + \alpha)/A_1]$
C20A-4	$V_{off} = V_{off1} + [V_{off2}(1 + \alpha)/(A_1 + \alpha)$

Figure 3-24 Effect of Individual OA's Offset Voltage on the C20As Input Offset Voltage

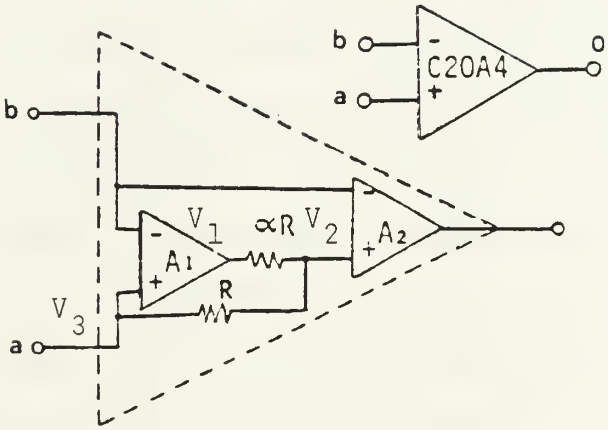


Figure 3-25 Schematic for C20A4 Used to Derive Offset Voltage Relationship

But, $V_2 = V_{off}$ and V_{off} for the circuit is V_3, so,

$$V_{off} = V_{off1} + V_{off2} \left(\frac{1+\alpha}{A_1+\alpha}\right)$$

To perform an offset voltage analysis to demonstrate the validity of the assertion that the offset voltage of the C2OA is determined by the offset voltage of the A1 OA required the design to two OAs with different offset voltages. One of these two OAs used was the basic LM741 model. Its voltage offset was found to be 0.15 mV. A second model was created by using resistors in the emitters of the input stage transistors Q1 and Q2. Its offset was found to be 0.916 mV. The program of Appendix O was used to obtain these results. The four possible combinations of these two OAs were then considered in a C2OA3 inverting amplifier configuration. The results of a computer analysis of this configuration are shown in Figure 3-26. It can be seen from these results that the offset of the C2OA3 is controlled by the offset of the A1 amplifier. Appendix P shows the computer program used to generate these results.

Finally, an experiment was performed in the laboratory to show that a high speed, high accuracy OA could be produced by combining the best characteristic of two seperate OAs. A high speed OA(HA-2525) and a high accuracy OA(HA-5170) were combined in a C2OA4 configuration. The experimental results are shown in Figure 3-27 and conslusively support the hypotheses previously proven.

A1	A2	V_{OFF}(mV)
1	1	0.151
1	2	0.151
2	1	0.916
2	2	0.917

Note: V_{OFF}(OA #1) = 0.151 mV

V_{OFF}(OA #2) = 0.916 mV

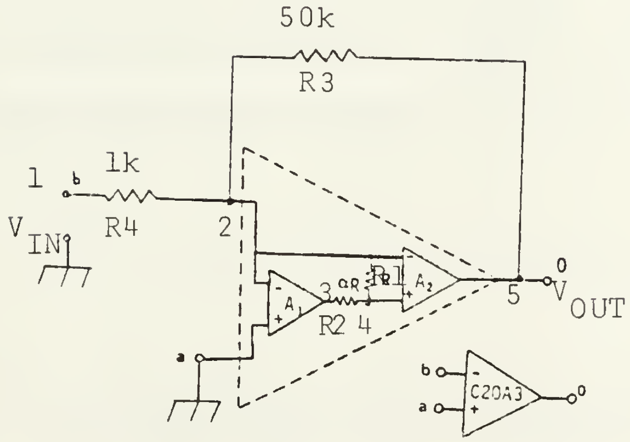


Figure 3-26 Computer Results of C20A3 Offset Voltage Analysis

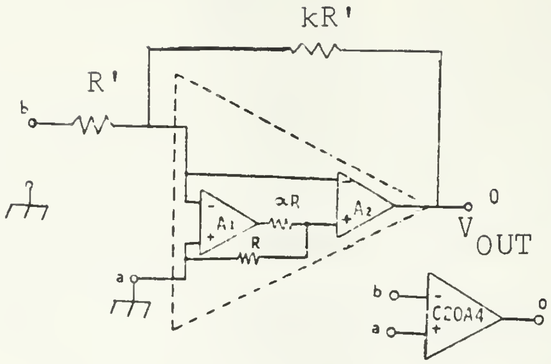
TRIAL I

$R=1.18\ k\Omega$

$\alpha R=3.88 k\Omega$

$R'=119\Omega$

$kR'=1.34kR$



TRIAL II

$R=246\Omega$

$\alpha R=4.8k\Omega$

$R'=119\Omega$

$kR'=246\Omega$

SINGLE OA		SR (V/μsec)	V_{OFF}
HA-2525	#1	140.8	6.68 mV
HA-5170	#2	8	121 μV

TRIAL	C20A4		(V/μsec)	V_{OFF}
	A1	A2		
I	1	2	6.25	6.7 mV
II	2	1	142.9	53 μV

Figure 3-27 Experimental Results for C20A4 with a High Accuracy OA and a High Speed OA

F. CONCLUSIONS

The C2OA has been shown to be a superior extended bandwidth Operational Amplifier. In addition to its extended bandwidth characteristics it has been shown to perform with a high degree of stability and low sensitivity to circuit element variations. It overcomes the disadvantages imposed by previous methods of active and passive compensation to extend the frequency dependent bandwidth. Additionally, the C2OA has been shown to overcome the offset problem associated with attempts to enhance the speed of the OA. It has been verified by computer simulation, theoretical, and experimental results that a high accuracy, high speed OA can be produced by using the C2OA. These results are better than those offered by state-of-the-art designs. An additional advantage of the CNOA is that it may be implemented using current technology. Although this chapter has considered only the C2OA, the results may be extended to the C3OA and C4OA.

IV. USE OF THE CNOA IN ACTIVE-RC FILTERS

A. BACKGROUND

It has been shown in Chapter III that the CNOA provides an Operational Amplifier with far better characteristics than the single OA, namely, extended bandwidth, lower sensitivity to circuit element variations, better stability, and the capability to achieve a realization with both high speed and high accuracy. This chapter will show the application of the CNOA to active-RC filters.

Many different technologies exist for realizing filters. Perhaps the oldest of these is where inductors, capacitors, and resistors are used in a passive RLC network. The major drawback of this is that in low frequency applications (dc to 100 kHz), inductors are extremely bulky and their non-ideal characteristics greatly hinder the filter performance. Further, inductors have the added disadvantage that they cannot be fabricated utilizing IC technology. The RC filter provides an alternative to this filter containing an inductor. The simple RC filter is realized through the combination of a resistor and a capacitor. The selectivity of this filter is limited, however, since its poles lie on the negative real axis in the s-plane. Utilizing active components in this filter can improve the selectivity of this filter by moving the circuit poles from the axis to complex locations in the s-plane [Ref. 14]. This chapter will consider CNOAs as the active elements in these "active-RC" filters. Specific filters which will be considered are the Multiple Feedback (MFB) Biquadratic (BIQUAD) Filter and the Generalized Immittance Converter (GIC).

B. THE MULTIPLE FEEDBACK (MFB) BIQUAD FILTER

The MFB Filter considered here utilizes a single OA and is shown in a Bandpass (BP) configuration. Figure 4-1 shows a schematic diagram of this filter. The BP transfer function of this filter is given by the following expression [Ref. 2: p. 83]:

$$H_i(s)=\frac{k}{1+k}\frac{1}{R_1C_1}\cdot\frac{s}{s^2+s\left(\frac{1}{1+k}\right)\left(\frac{1}{R_1C_1}+\frac{1}{R_2C_2}+\frac{1}{R_2C_1}\right)+\left(\frac{1}{1+k}\right)\left(\frac{1}{R_1R_2C_1C_2}\right)}$$

For $R_1=R_2=R$, $C_1=C_2=C$, and $\omega=\frac{1}{RC}$.

$$\frac{V_{OUT}}{V_{IN}} = -k\,\frac{s/\omega}{1 + 3\,s/\omega + (1+k)\,s^2/\omega^2}$$

Since the general expression for a BP transfer function is given by

$$H(s) = \frac{a_1 s}{s^2+s(\omega_o/Q)+\omega_o^2}$$

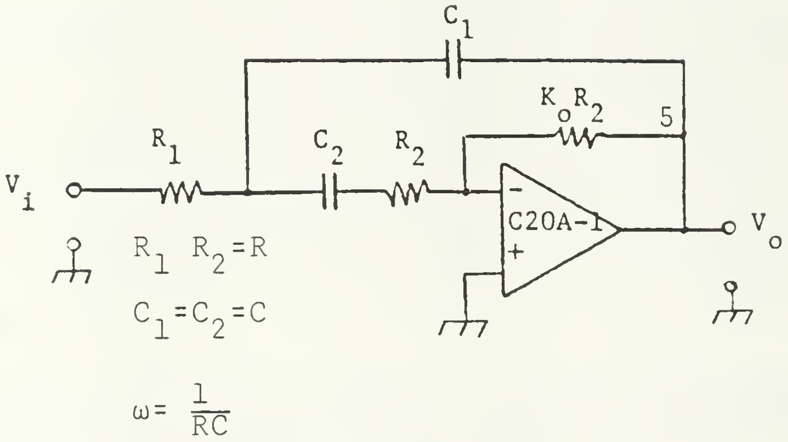


Figure 4-1 The MFB Single-BIQUAD BP Filter Using a C20A1

then for the filter being considered

$$\omega_o = \omega/\sqrt{1+k}$$

$$Q_p = \sqrt{1+k}/3$$

$$BW = 3\omega_o/\sqrt{1+k}$$

where ω_o is the filter poles resonant frequency and Q_p is the quality factor.

Figures 4-2, 4-3, and 4-4 show computer results for the freqyency response of an MFB using both the single OA and a C2OA 1. The schematic of Figure 4-1 was used in the design of these filters. The design center frequencies of the filters shown are 6.25 kHz, 40 kHz, and 100 kHz, respectively. Additionally, the filter for each design f_o is plotted using ideal OAs for the C2OA 1. It should be noted that for the C2OA the resistor-ratio, α, can be used to control the amplitude and the transfer function at resonant frequency of the filter, as well as the quality factor Q_p. The effects of adjusting α are shown in Figure 4-5 for a design of f_o = 60 kHz. Figure 4-6 shows the effects on the C2OA 1 response caused by a ±5% resistor-ratio variation (small, as compared to the variation used to adjust f_o) and Figure 4-7 shows the effects of power supply voltage variations. The response for the ±5% curves are so close

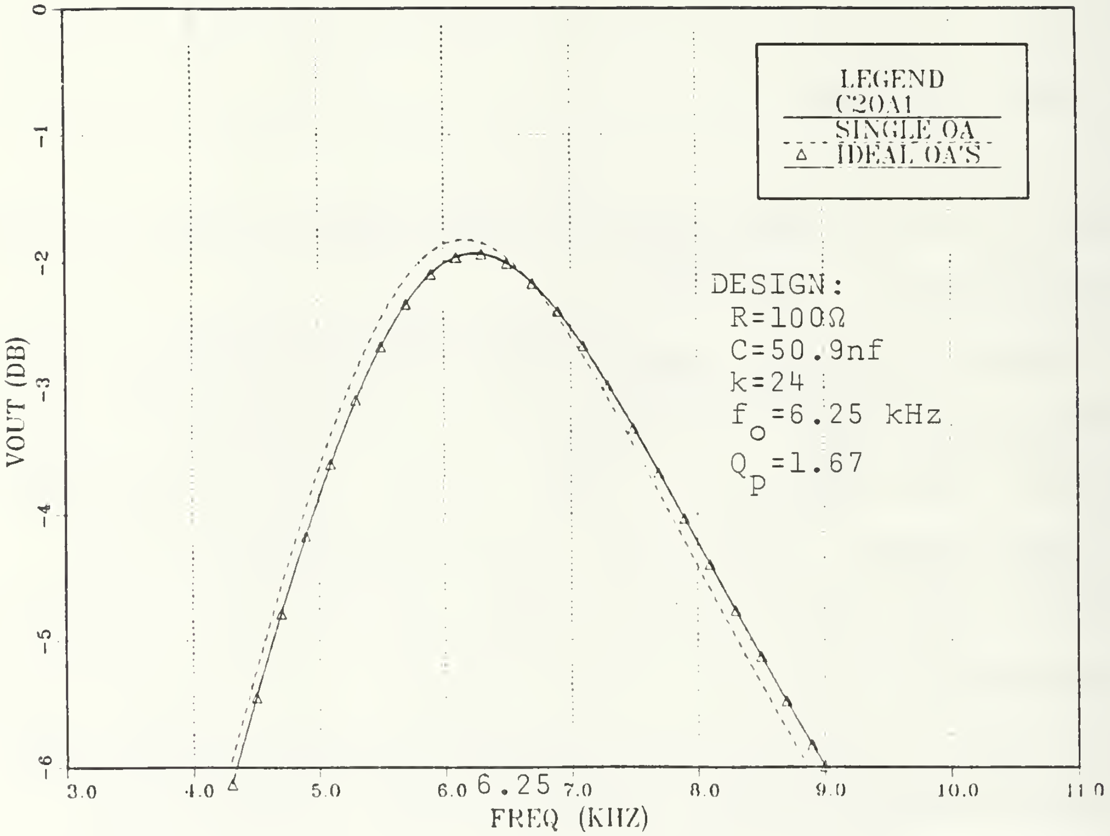


Figure 4-2 Frequency Response of MFB BIQUAD (f_o=6.25 kHz)

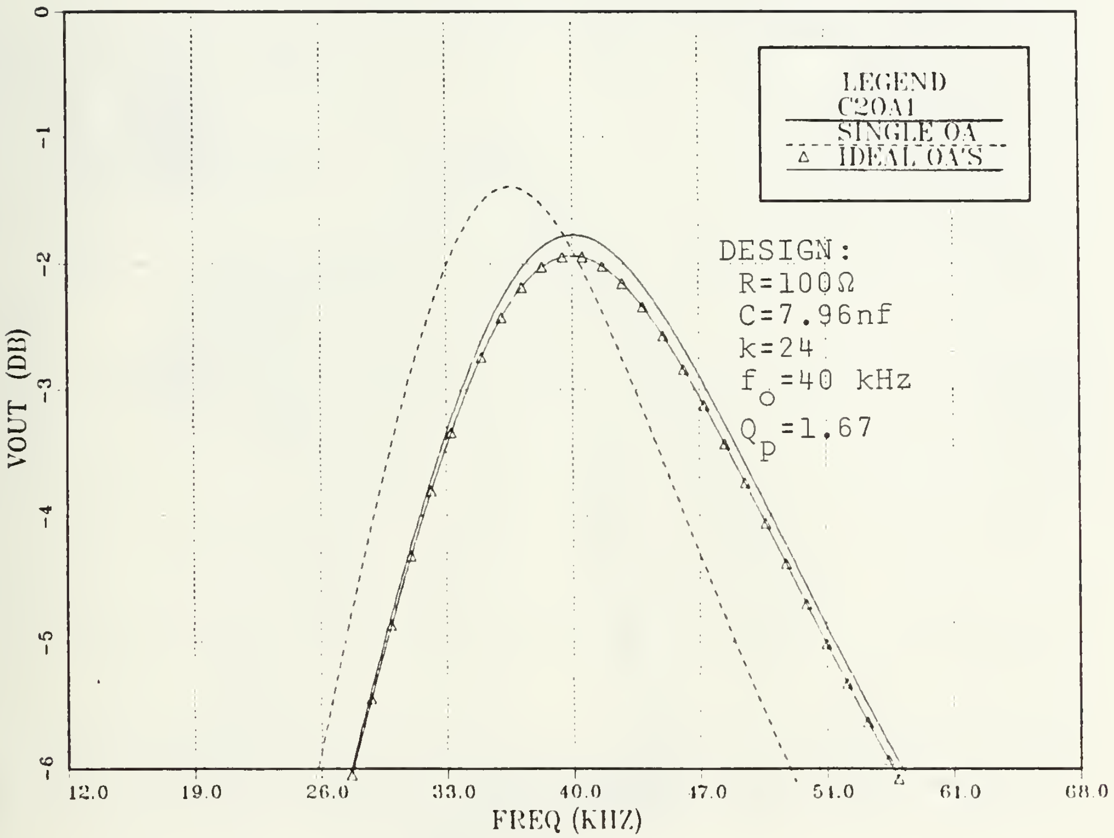


Figure 4-3 Frequency Response of MFB BIQUAD (f_o=40 kHz)

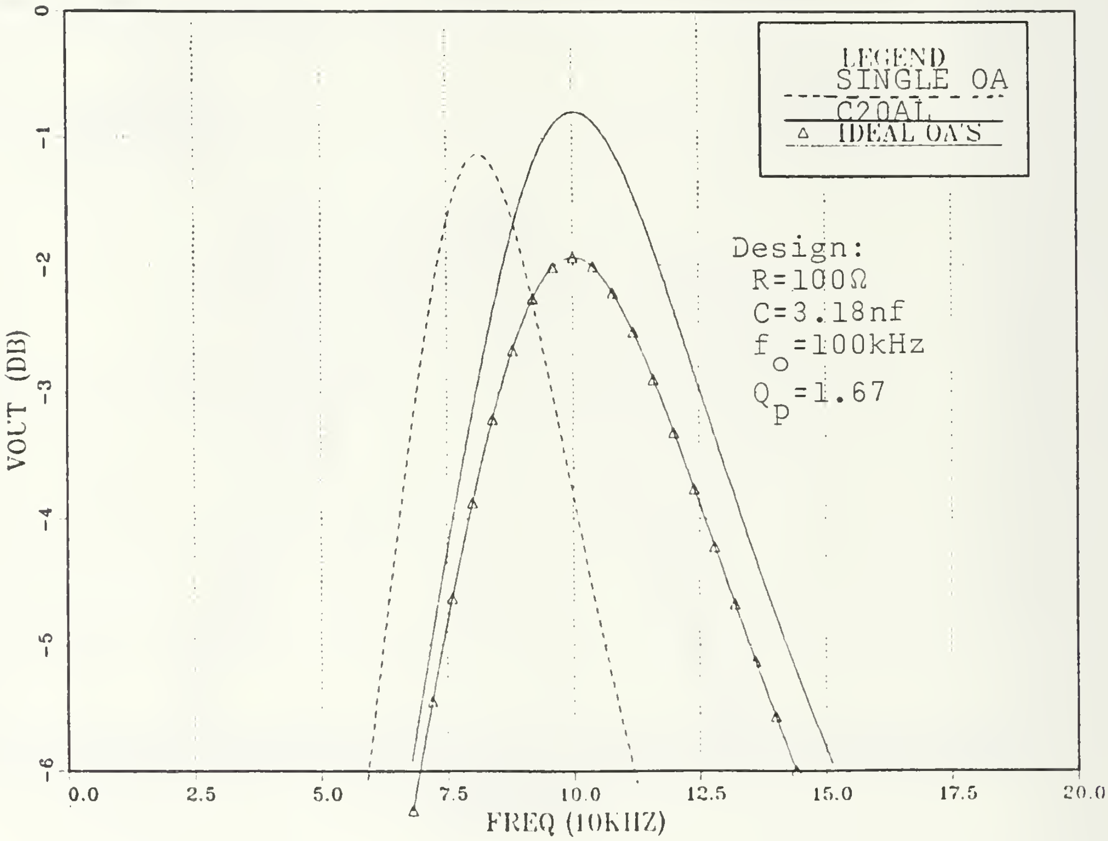


Figure 4-4 Frequency Response of MFB BIQUAD (f_o=100 kHz)

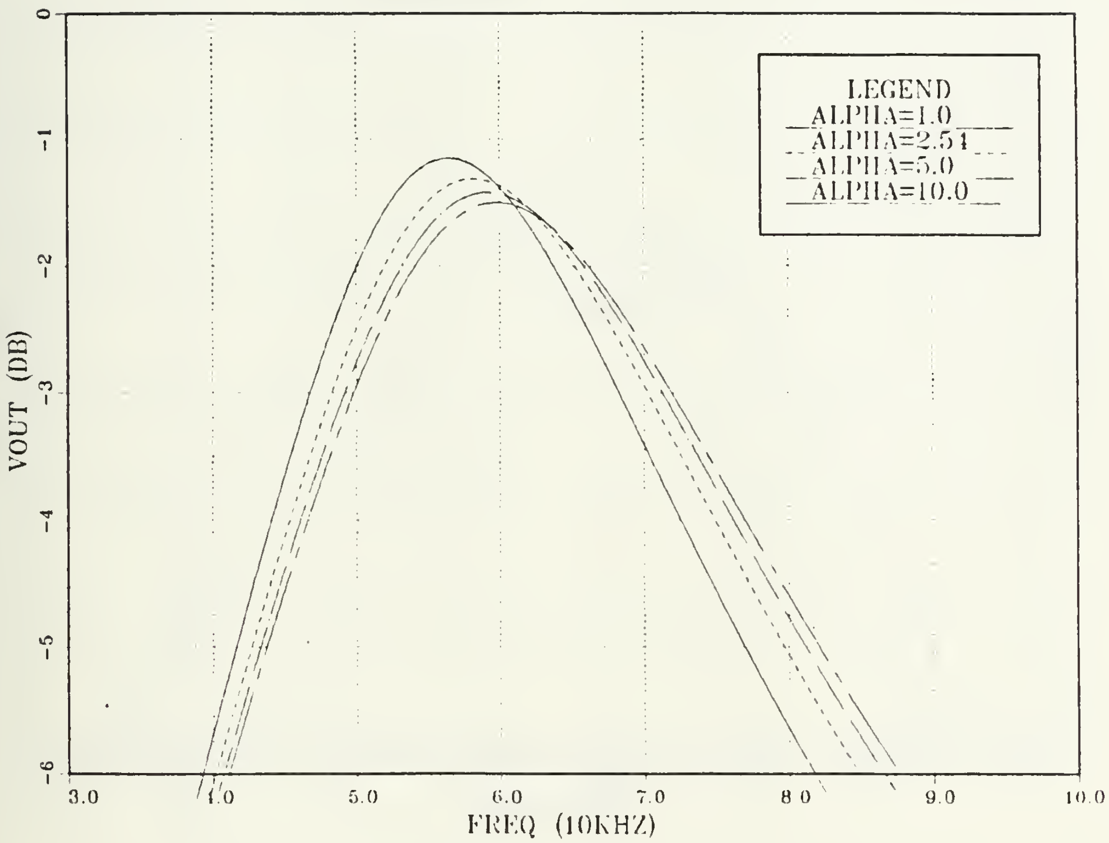


Figure 4-5 Frequency Response of MFB BIQUAD (f_o=60 kHz) Showing the Effects of Varying α

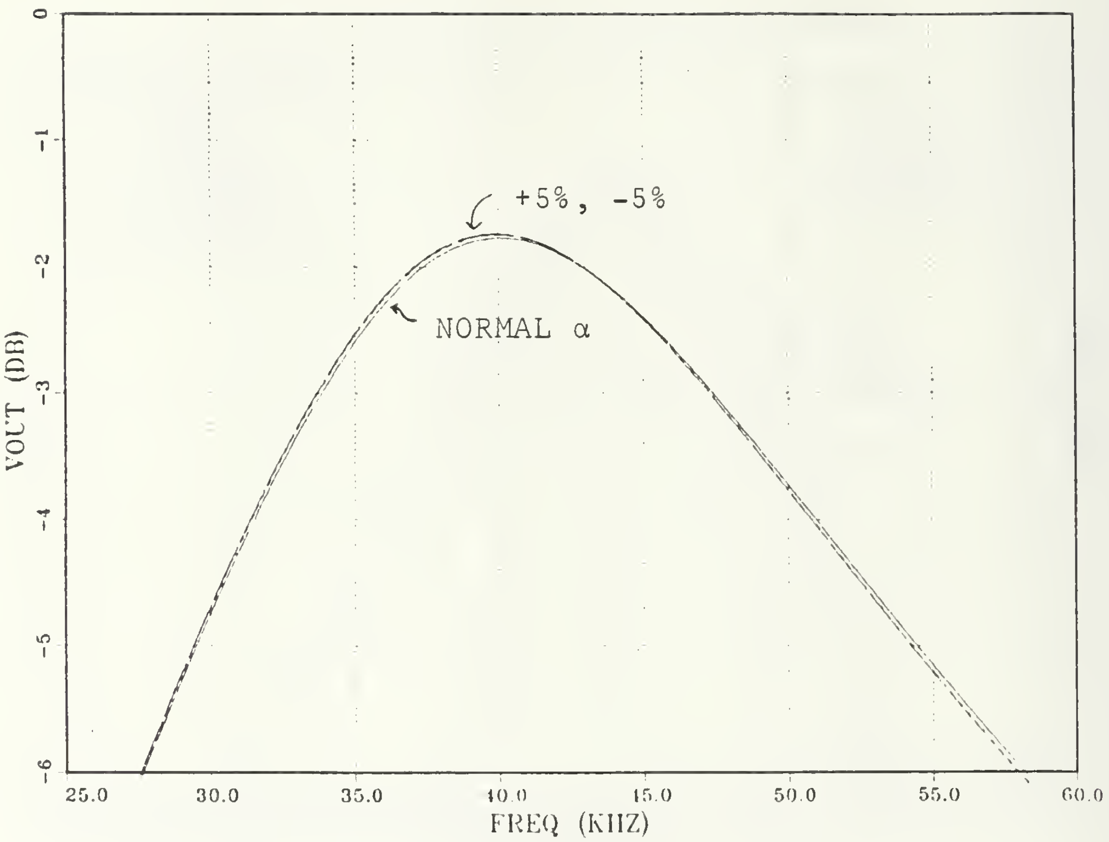


Figure 4-6 Effects of Small Resistor-Ratio (α) Variation on Frequency Response of MFB BIQUAD (f_o=40 kHz)

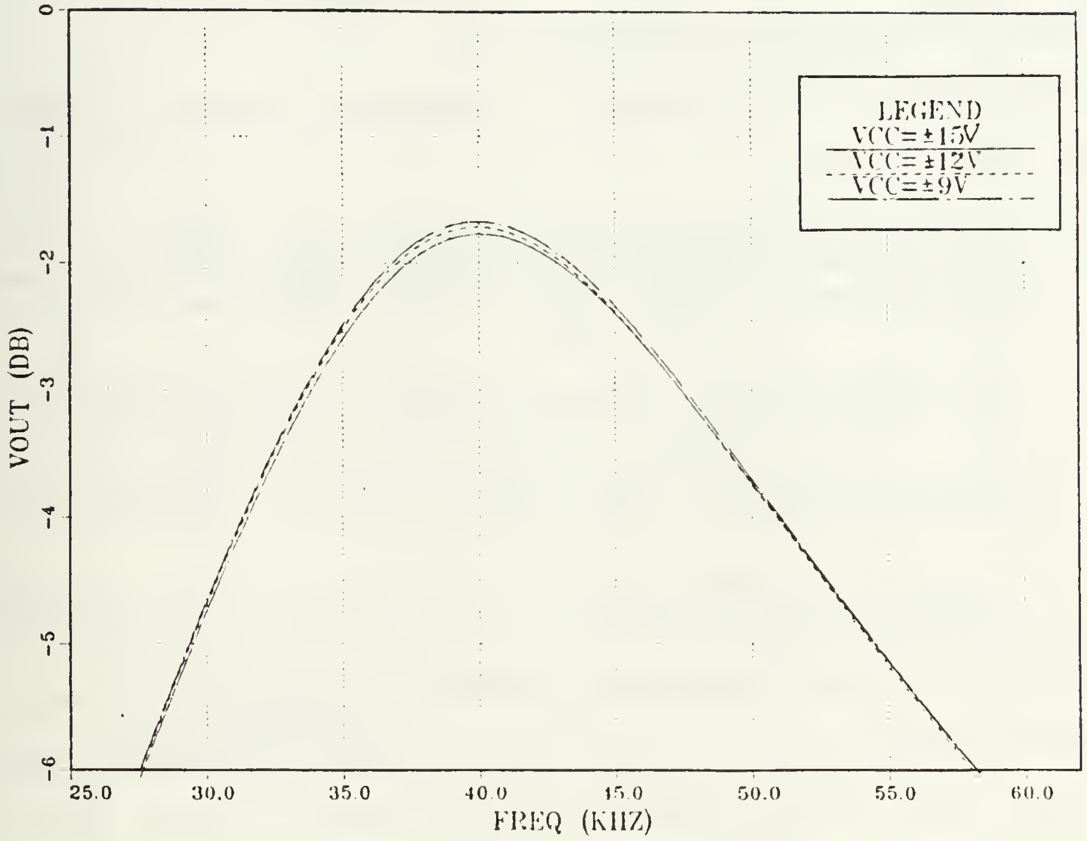


Figure 4-7 Effects of Power Supply Voltage Variation on Frequency Response of MFB BIQUAD (f_o=40 kHz)

that they appear as one curve in Figure 4-6. Figure 4-8 shows the comparisons of Q_p and f_o variations from design from the C20A1 vs. the single OA. Appendices P, Q, and R contain the computer programs used to generate the results obtained in Figures 4-2 through 4-8.

An analysis of the computer results for the MFB BIQUAD shows the following:

1. The C20A1 corresponds much closer to the ideal response than the single OA in all cases. At the lower frequencies the C20A1 very closely approximates the response of the ideal case.
2. The actual quality factor (Q_p) and resonant frequency (f_o) are very close to design for the C20A1.
3. The C20A1 displays a low sensitivity to variation in circuit elements.
4. The C20A1 is shown to operate acceptably with variations in power supply voltage.

There was some discrepancy between the anticipated and computer results for the single OA. It was envisioned that the amplitude of the response for the single OA would drop off at higher frequencies, but it was not the case. This discrepancy also affected the C20A1 to a lesser extent, but it is felt that the general results obtained were still valid. It is believed that this discrepancy is due to the high degree of complexity of the model utilized. The above results demonstrate clearly the advantage of using a C20A in place of a single OA in active filters.

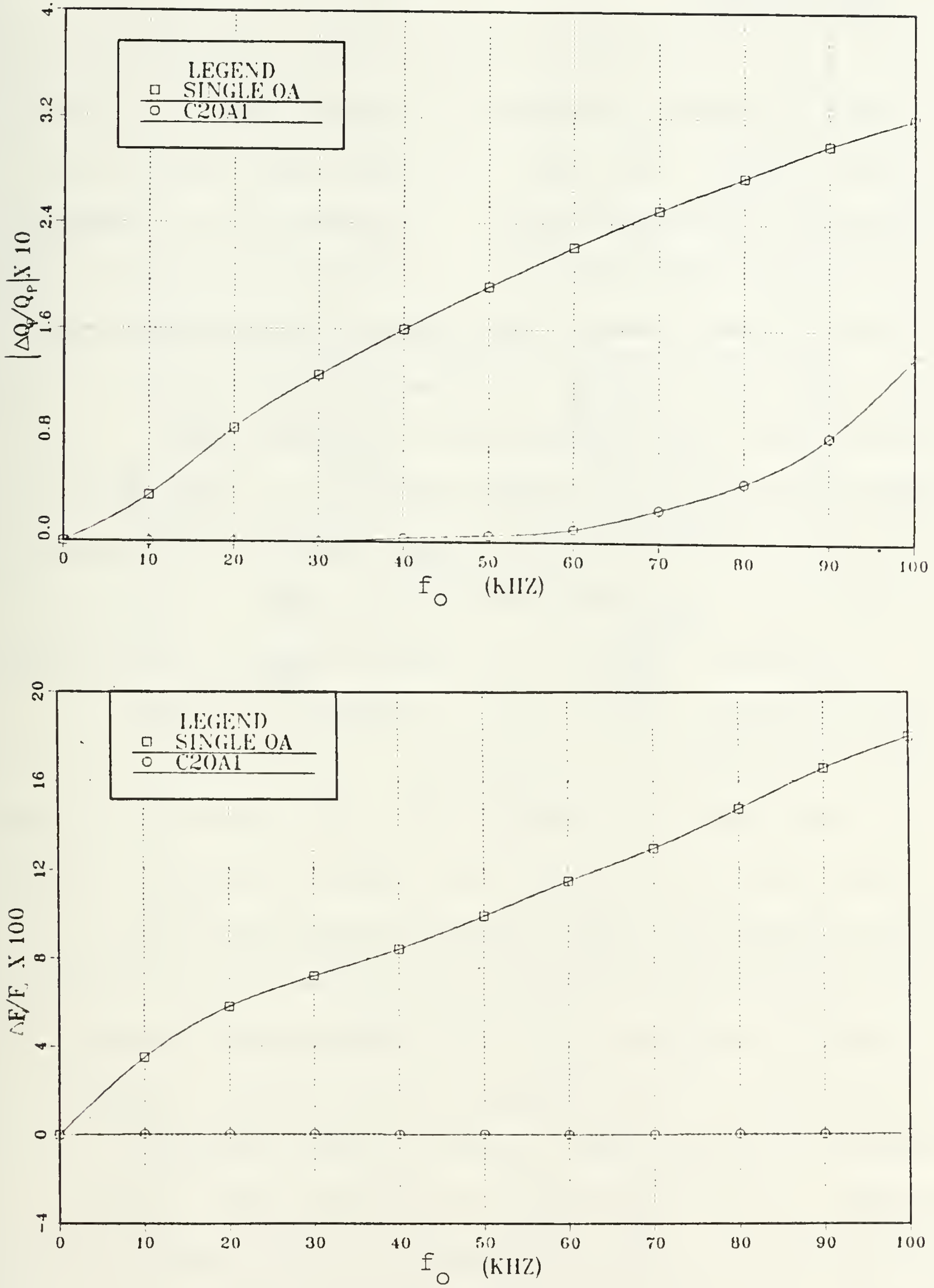


Figure 4-8 Comparison of Q_p and f_o Variations (vs. f_o) for Single OA and C20A1 Used in MFB BIQUAD Filters

C. HIGH FREQUENCY GENERALIZED IMMITTANCE CONVERTERS (GICs) USING CNOA'S

It was mentioned in the introduction to this chapter that the use of inductors in filters is impractical due to their bulk and expense. One way to overcome this problem is to design and inductorless filter. One method is to simulate the LC network associated with a filter through use of the active-RC filter. One of the promising designs that can affect this simulation is the Generalized Immittance Converter [Ref. 15]. This design maintains a low sensitivity to circuit element variations and possesses a high degree of stability. The same bandwidth limitations imposed by the non-ideal performance of the OA effect the GIC. Once again, however, the CNOA provides an alternative to help overcome this problem. A schematic for this filter is contained in Figure 4-9.

To show the use of CNOAs in the GIC, the BP realization of Figure 4-10 was selected. As shown, it utilizes a C20A3 as the A1 amplifier and a C20A4 as the A2 amplifier. Circuit parameters shown are for a design of $f_o = 20$ kHz. The computer simulation for this configuration is shown in Figure 4-11. Also contained in that figure is the response corresponds very closely to the theoretical response. As was the case with the MFB filter, α was used to control f_o and the amplitude of the response of the filter. Figure 4-12 shows the effect of a ±5%

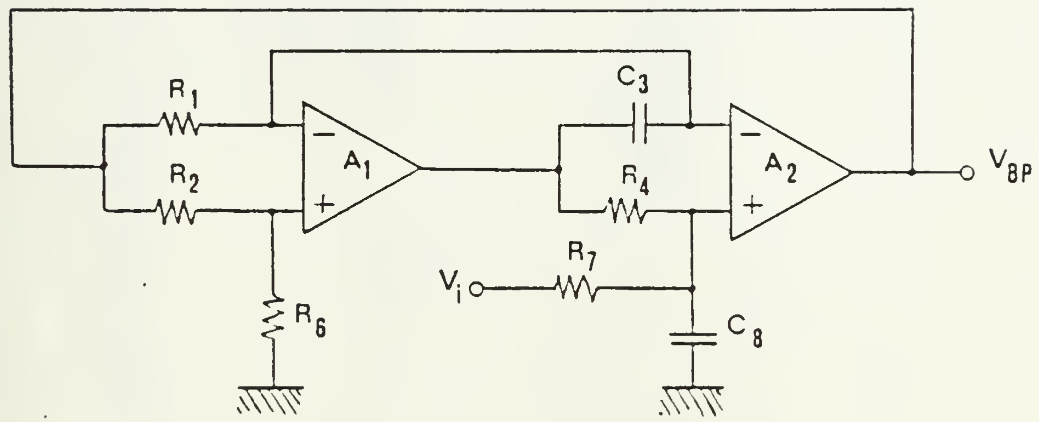
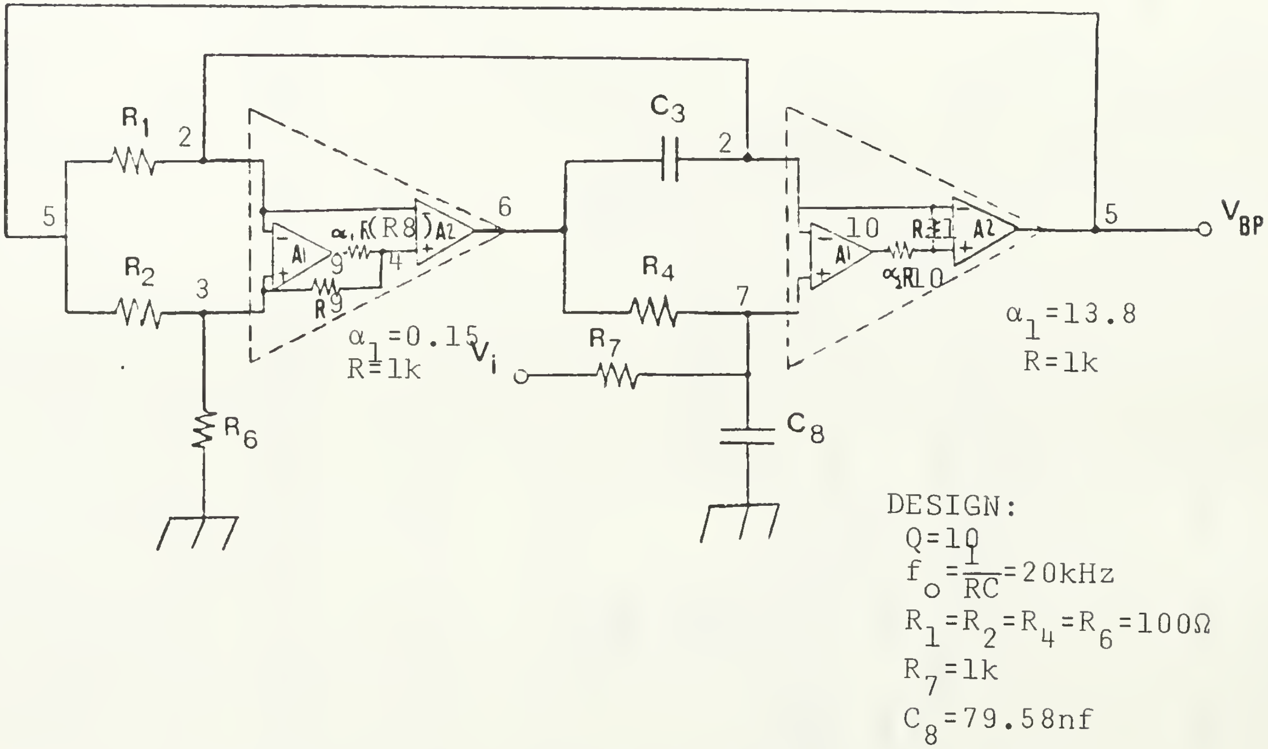


Figure 4-9 BP Filter Realization of GIC Using Single OAs



DESIGN:
Q=10
$f_o=\frac{1}{RC}$=20kHz
$R_1=R_2=R_4=R_6=100\Omega$
R_7=1k
C_8=79.58nf

Figure 4-10 Practical BP Filter Realization of the Composite GIC Using C20A4 and C20A3

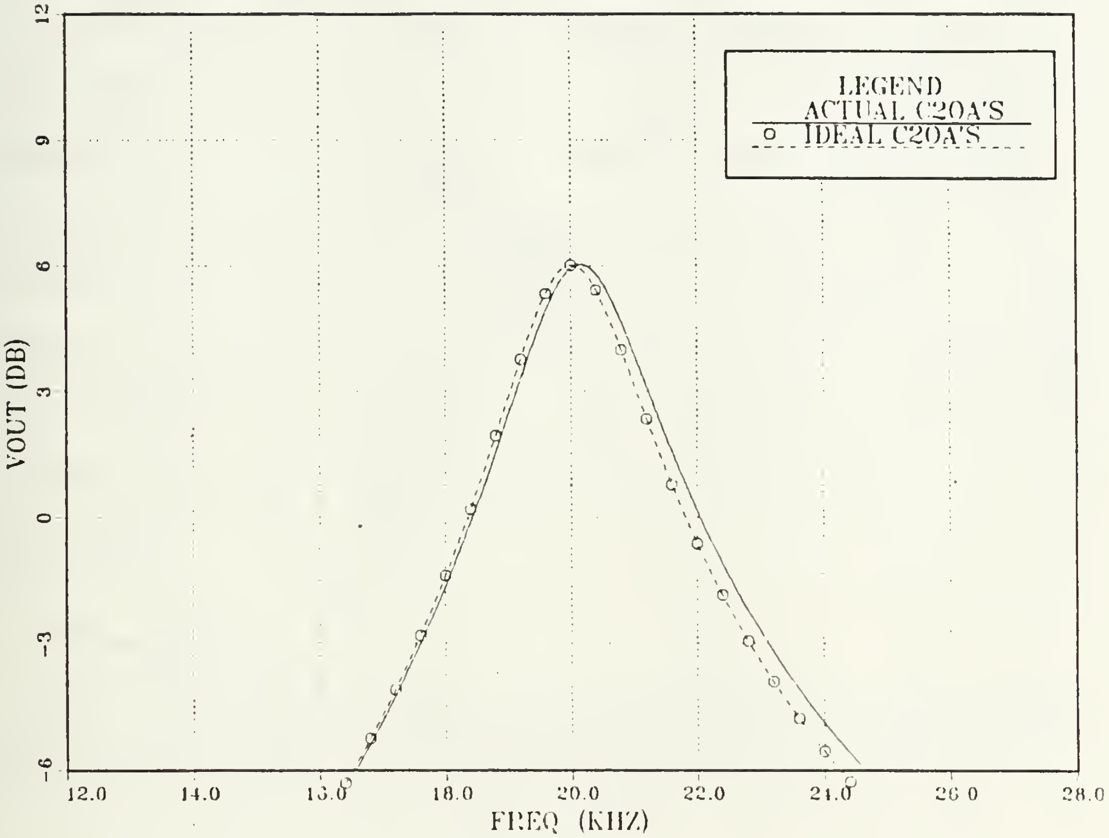


Figure 4-11 Frequency Response of GIC BP Filter Using C20A4 and C20A3 (f_o=20 kHz)

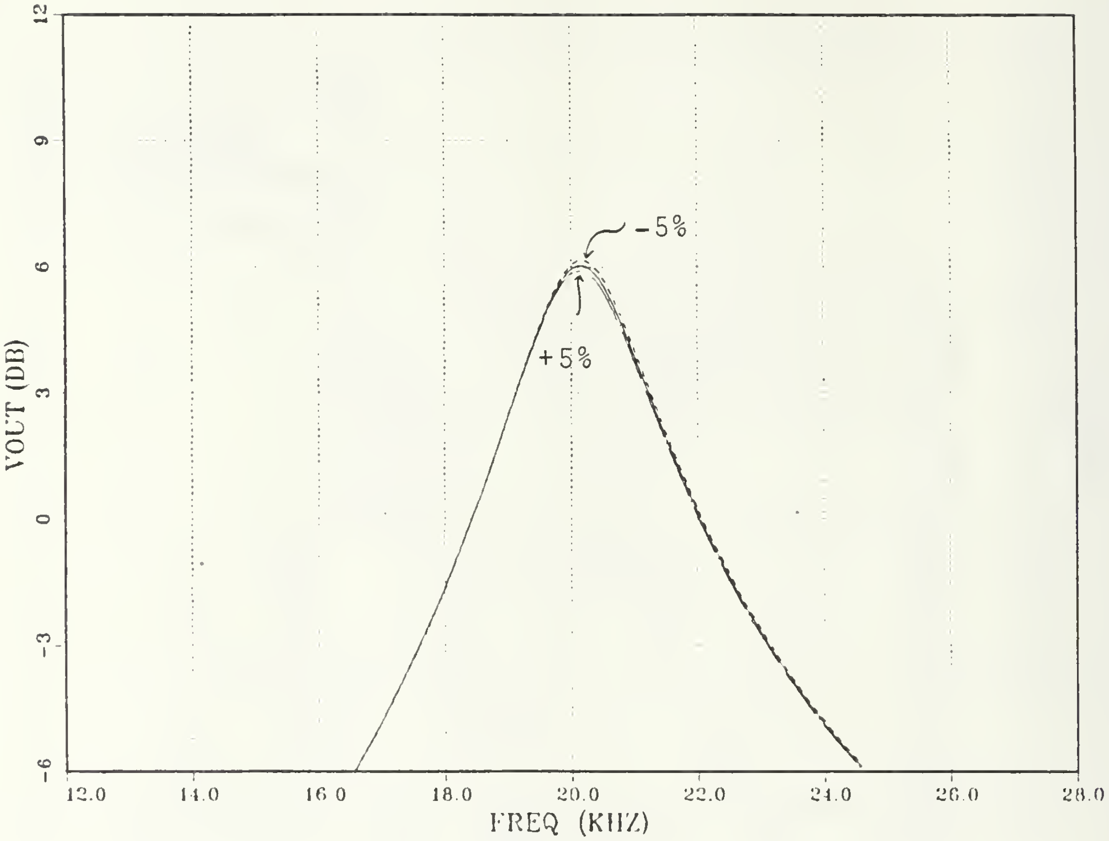


Figure 4-12 Effects of Resistor-Ratio Variation on Frequency Response of GIC BP Filter (f_o=20 kHz)

resistor-ratio variation on the response of the filter and it can be seen from that figure that the filter is relatively insensitive to those small variations. Figure 4-13 shows that the filter can operate acceptably with lower than normal power supply voltages. The response of the single OA used in place of the CNOA is this configuration was not considered to satisfactorily represent the situation and as such was omitted. The program of Appendix S was utilized to produce the computer results for the GIC Filter and the program of Appendix T was used to produce the frequency response for the filter using ideal OAs.

D. CONCLUSIONS

This chapter has shown the application of the extended BW CNOA to active-RC filters. It has been shown that the response of these filters very closely approximate the ideal at low frequencies and that the filters are relatively insensitive to small variations in resistor-ratio variations and variations in power supply voltages. Further, it has been shown how the resistor-ratio can be used to control the resonant frequency and amplitude of the filters. These filters represent but a small number of potential applications for the CNOAs.

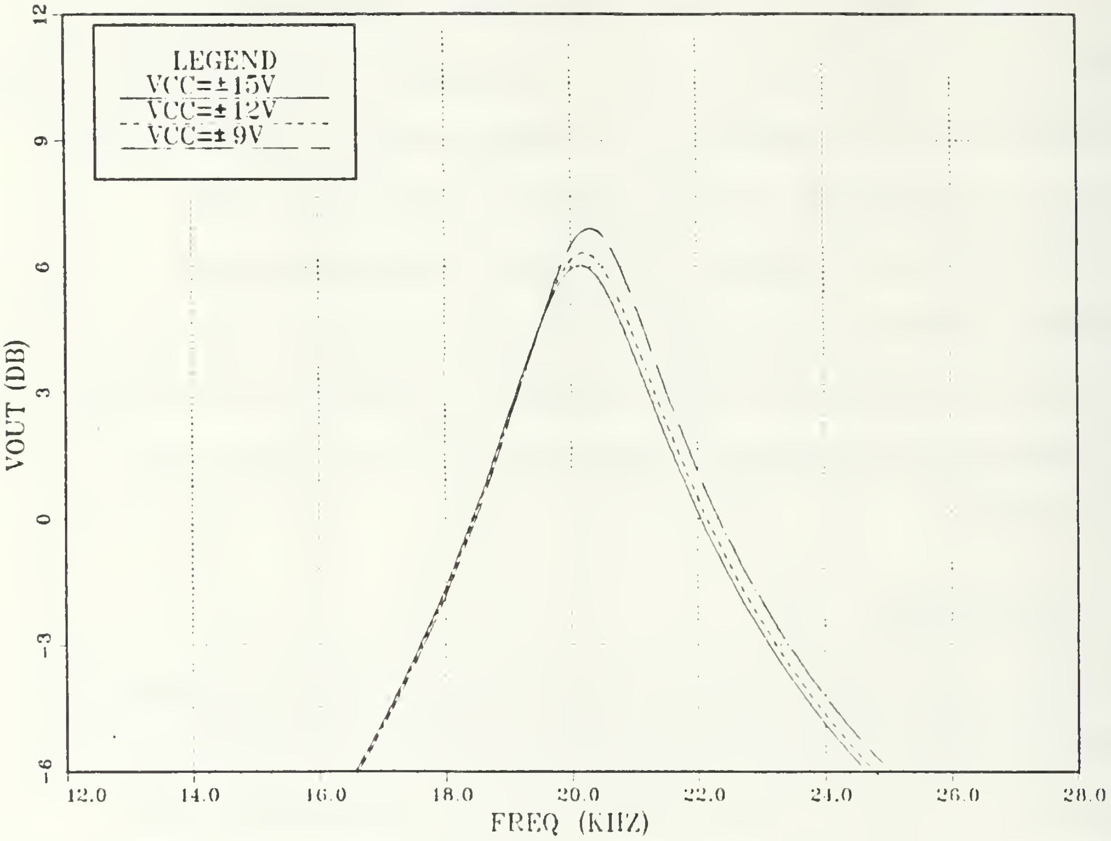


Figure 4-13 Effects of Power Supply Variation on Frequency Response of GIC BP Filter (f_o=20 kHz)

V. CONCLUSIONS

The objective of this research was to introduce a unified approach to several of the problems associated with Operational Amplifiers (OAs), namely, frequency dependent gain, and speed and accuracy limitations. The method introduced to solve these problems was the Composite Operational Amplifier (CNOA), where N=2, 3, or 4 single OAs. This device is treated as a single OA and is shown to possess the same versatility as the single OA. Its characteristics have been shown to be superior to the single OA and it has been shown to overcome the disadvantages associated with previous attempts to extend BW and improve slew rate. A combination of computer simulation, theoretical, and experimental results were used to generate the findings of the research.

Chapter I discussed the problems of the high frequency rolloff of the OA and the limitations imposed in attempts to improve slew rate. Chapter II introduces the model utilized to generate the computer simulation results of this paper. Chapter III discusses the generation of the CNOA and contains the computer, theoretical, and experimental results which demonstrate the superiority of the CNOA. Chapter IV shows the application of the CNOA to active-RC filters.

Current passive and active compensation introduced to minimize the high frequency rolloff problem of the OA have been found to be in most cases impractical or not cost justified. Furthermore, each of these methods was introduced for specific applications and a general approach for different circuit networks was not found. These methods have included the introduction of passive components to produce an amount of phase lead to compensate for the phase lag due to the imperfect OAs, adding additional OAs to a configuration, and the production of wider GBWP OAs. It was shown theoretically and verified by computer simulation that the C2OA finite gain amplifier has a greatly extended BW over the single OA, or cascaded stages of OAs. Additionally, the C2OA was shown to have a high degree of stability and a low sensitivity to circuit element variations when compared with the state-of-the-art designs.

It was shown that each of the common methods presently available for enhancing slew rate contributed to an offset problem. These methods included the use of JFETs in the OA differential input stage circuitry, the inclusion of emitter degeneration resistors in the emitters of the transistors which form the input stage, increasing the OA GBWP, and increasing the charging current available to the internal compensating capacitor through alternative routes. The use of the C2OA, however, was shown to be a method whereby a high slew rate could be attained with low offset voltage. This is accomplished by using a low offset OA as the input OA (A1) of the configuration and a high slew rate OA as the output OA (A2) of the configuration. The use of such different OAs in constructing the CNOAs was possible due to the fact that mismatching of individual OA's GBWPs is tolerable in these proposed families of CNOAs. This provided an excellent chance to construct composite OAs tailored to certain unique specifications such as high speed and high accuracy. These improved specifications were proven through the use of computer, theoretical, and experimental results. An application of the CNOA was shown in active-RC filters and it was demonstrated that these devices performed considerably better with the CNOA than with the single OA.

The computer model used to generate the computer simulation results operated satisfactorily for most of the research, however, some difficulties were experienced. As noted, a problem with slew rate analysis was experienced during verification of the basic model and then later a problem with the response of a single OA in an active filter configuration was experienced. Additionally, some sensitivity of the SPICE Program to the method in which values of components were input was experienced. Attempts were made to adjust the system tolerance values, but were to no avail. It is recommended that prior to further research requiring OA circuit analysis an attempt be made to obtain a full set of transistor parameters for inclusion in the SPICE program. Attempts to obtain a complete set of parameters for specific OAs was not successful and as such most values were allowed to default to system assigned values. The lack of these parameters, coupled with the high degree of sophistication of the model is believed to have contributed to some of the difficulties experienced with SPICE. Consideration should also be given to utilizing a more simple model for the single OA. Finally, it is recommended that the 2G Version of SPICE resident on the IBM 3033, and utilized in this research, be compared to later versions of the program to ascertain the extent to which problems associated with the 2G Version hinder circuit analysis efforts.

In conclusion, the objective of this research has been met. The CNOA has been shown to be a unified approach to overcoming the frequency dependent gain problem, the speed problem, and the accuracy problem associated with the Operational Amplifier. An added advantage of this device is that it is fully compatible with state-of-the-art IC technology and as such requires no new technological innovation.

APPENDIX A

PROGRAM FOR THE BASIC LM741 SIMULATION MODEL

```
*****************************
*                           *
*        LM741 OP AMP       *
*        BASIC MODEL        *
*                           *
*****************************


*THIS IS THE MODEL UTILIZED TO SIMULATE THE LM741 OP AMP
*IT MAY BE CONFIGURED TO MODEL VARIOUS CIRCUITS INCLUDING
*POSITIVE AND NEGATIVE FINITE GAIN AMPLIFIERS, ACTIVE
*FILTERS, AND COMPOSITE OPERATIONAL AMPLIFIERS


 .WIDTH IN=80 OUT=80
 .OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

 VCC  1  0      15
 VEE 26  0     -15
 Q1  12  0  8   MOD2
 Q2  12 14  7   MOD2
 Q3  10  6  8   MOD1
 Q4  15  6  7   MOD1
 Q5  10 13 11   MOD2
 Q6  15 13 16   MOD2
 Q7   1 10 13   MOD2
 Q8  12 12  1   MOD1
 Q9   6 12  1   MOD1
 Q10  6  3  4   MOD2
 Q11  3  3 26   MOD2
 Q12  2  2  1   MOD1
 Q13 17  2  1   MOD3
 Q14  1 17 22   MOD5 3
 Q15 17 22 19   MOD2
 Q16  1 15  9   MOD2
 Q17 18  9 25   MOD2
 Q18 17 20 21   MOD2
 Q19 17 17 20   MOD2
 Q20 26 21 23   MOD6 3
 Q21 24 23 19   MOD1
 Q22 15 24 26   MOD2
 Q23 26 18 21   MOD1
 Q24 24 24 26   MOD2
 Q25 18  2  1   MOD4
 R1  11 26 1K
 R2  16 26 1K
 R3  13 26 50K
 R4   4 26 5K
 R5   2  3 39K
 R6  22 19 27
 R7  19 23 27
 R8  25 26 100
 R9   9 26 50K
 R10 20 21 40K
 R11 24 26 50K
 C1  15 18 30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.END
```

APPENDIX B

PROGRAM FOR LM741 INVERTING AMPLIFIER FREQUENCY AND PHASE RESPONSE

```
******************************
*                            *
* LM741 INVERTING AMPLIFIER  *
*                            *
******************************


*THIS IS THE MODEL UTILIZED TO SIMULATE THE LM741 OP AMP
*IN A FINITE GAIN INVERTING AMPLIFIER CONFIGURATION; IT
*DETERMINES AMPLITUDE AND PHASE RESPONSE

 .WIDTH IN=80 OUT=80
 .OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

 VCC  1  0     15
 VEE 26  0    -15
 Q1  12  0   8   MOD2
 Q2  12 14   7   MOD2
 Q3  10  6   8   MOD1
 Q4  15  6   7   MOD1
 Q5  10 13  11   MOD2
 Q6  15 13  16   MOD2
 Q7   1 10  13   MOD2
 Q8  12 12   1   MOD1
 Q9   6 12   1   MOD1
 Q10  6  3   4   MOD2
 Q11  3  3  26   MOD2
 Q12  2  2   1   MOD1
 Q13 17  2   1   MOD3
 Q14  1 17  22   MOD5 3
 Q15 17 22  19   MOD2
 Q16  1 15   9   MOD2
 Q17 18  9  25   MOD2
 Q18 17 20  21   MOD2
 Q19 17 17  20   MOD2
 Q20 26 21  23   MOD6 3
 Q21 24 23  19   MOD1
 Q22 15 24  26   MOD2
 Q23 26 18  21   MOD1
 Q24 24 24  26   MOD2
 Q25 18  2   1   MOD4
 R1  11 26 1K
 R2  16 26 1K
 R3  13 26 50K
 R4   4 26 5K
 R5   2  3 39K
 R6  22 19 27
 R7  19 23 27
 R8  25 26 100
 R9   9 26 50K
 R10 20 21 40K
 R11 24 26 50K
 R12 14  5  1K
 R13 19 14  10K
 C1  15 18 30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
VIN  5  0  AC 0.1
.AC DEC 14 1 3MEG
.PRINT AC VDB(19)  VP(19)
.PLOT  AC VDB(19)  VP(19)
.END
```

APPENDIX C

PROGRAM FOR LM741 NON-INVERTING AMPLIFIER FREQUENCY AND PHASE RESPONSE

```
**********************************
*                                *
* LM741 NON-INVERTING AMPLIFIER *
*                                *
**********************************


*THIS CIRCUIT SIMULATES A NON-INVERTING AMPLIFIER;IT IS
*USED TO DETERMINE AMPLITUDE AND PHASE RESPONSE

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7


**SUBCIRCUIT DEFINITION


VCC  1  0     15
VEE 26  0    -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
R12 14  0  1K
R13 19  14 9K
C1  15 18 30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
VIN 5  0  AC  0.1
.AC DEC 15  1  1MEG
.PRINT AC   VDB(19)
.PLOT AC   VDB(19)
.END
```

APPENDIX D

PROGRAM FOR LM741 NEGATIVE SLEW RATE RESULTS

```
*****************************
*                           *
* LM741 INVERTING AMPLIFIER *
*                           *
*****************************


*THIS CIRCUIT SIMULATES AN LM741 UNITY GAIN FOLLOWER
*IT DETERMINES CIRCUIT SLEW RATE;ITS RESULTS DEMONSTRATE
*THE DIFFICULTY WITH THE BASIC MODEL EXPERIENCED WHEN
*TRANSISTOR JUNCTION CAPACITANCES ARE INCLUDED

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

VCC 1   0      15
VEE 26  0     -15
Q1  12   5   8   MOD2
Q2  12  19   7   MOD2
Q3  10   6   8   MOD1
Q4  15   6   7   MOD1
Q5  10  13  11   MOD2
Q6  15  13  16   MOD2
Q7   1  10  13   MOD2
Q8  12  12   1   MOD1
Q9   6  12   1   MOD1
Q10  6   3   4   MOD2
Q11  3   3  26   MOD2
Q12  2   2   1   MOD1
Q13 17   2   1   MOD3
Q14  1  17  22   MOD2 3
Q15 17  22  19   MOD2
Q16  1  15   9   MOD2
Q17 18   9  25   MOD2
Q18 17  20  21   MOD2
Q19 17  17  20   MOD2
Q20 26  21  23   MOD1 3
Q21 24  23  19   MOD1
Q22 15  24  26   MOD2
Q23 26  18  21   MOD1
Q24 24  24  26   MOD2
Q25 18   2   1   MOD4
R1  11  26  1K
R2  16  26  1K
R3  13  26  50K
R4   4  26  5K
R5   2   3  39K
R6  22  19  27
R7  19  23  27
R8  25  26  100
R9   9  26  50K
R10 20  21  40K
R11 24  26  50K
C1  15  18  30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F)
.MODEL MOD2 NPN(BF=200 IS=10F)
.MODEL MOD3 PNP(BF=50 IS=2.5F)
.MODEL MOD4 PNP(BF=50 IS=7.5F)
VIN   5  0  PULSE(5.0 -5.0 10US 1NS 1NS 60US 120US)
.TRAN 3US 290US
.PRINT TRAN V(19)
.PLOT TRAN V(19)
.END
```

APPENDIX E

PROGRAM FOR LM741 GOOD SLEW RATE RESULTS

```
                    *****************************
                    *                           *
                    * LM741 INVERTING AMPLIFIER *
                    *                           *
                    *****************************


*THIS CIRCUIT SIMULATES AN LM741 INVERTING AMPLIFIER
*IT DETERMINES CIRCUIT SLEW RATE

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

VCC 1  0      15
VEE 26 0     -15
Q1  12  0  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD2 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD1 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
R12 14  5 1K
R13  19 14 1K
C1  15 18 30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F)
.MODEL MOD2 NPN(BF=200 IS=10F)
.MODEL MOD3 PNP(BF=50 IS=2.5F)
.MODEL MOD4 PNP(BF=50 IS=7.5F)
VIN    5  0  PULSE(5.0 -5.0 10US 1NS 1NS 60US 120US)
.TRAN 1US 90US
.PRINT TRAN V(19)
.PLOT TRAN V(19)
.END
```

APPENDIX F

PROGRAM FOR OPEN LOOP FREQUENCY RESPONSE SIMULATION

```
******************************
*                            *
* LM741 INVERTING AMPLIFIER  *
*                            *
******************************


*THIS IS THE MODEL UTILIZED TO SIMULATE THE LM741 OP AMP IN A
*FINITE GAIN INVERTING AMPLIFIER CONFIGURATION;IT IS USED TO
*DETERMINE THE OPEN LOOP GAIN OF THE AMPLIFIER

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

VCC 1  0     15
VEE 26 0    -15
Q1  12 27  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
R12 14  5  1K
R13 19 14  93600K
R14 27  0  1K
C1  15 18 30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
VIN  5  0  AC  0.0000108
.AC DEC 14  1  3MEG
.PRINT AC VDB(19)  VP(19)
.PLOT  AC VDB(19)  VP(19)
.END
```

APPENDIX G

PROGRAM FOR DETERMINING TRANSISTOR COLLECTOR CURRENTS OF BASIC MODEL

```
*******************************
*                             *
* LM741 INVERTING AMPLIFIER   *
*                             *
*******************************

*THIS IS THE MODEL UTILIZED TO SIMULATE THE LM741 OP AMP IN A
*FINITE GAIN INVERTING AMPLIFIER CONFIGURATION;ITS PURPOSE
*IS TO MONITOR VARIOUS TRANSISTOR COLLECTOR CURRENTS

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

VCC 1   0     15
VEE 26  0    -15
Q1  27  35  8  MOD2
Q2  28  14  7  MOD2
Q3  10   6  8  MOD1
Q4  15   6  7  MOD1
Q5  10  13 11  MOD2
Q6  15  13 16  MOD2
Q7   1  10 13  MOD2
Q8  12  12  1  MOD1
Q9  32  12  1  MOD1
Q10 32   3  4  MOD2
Q11  3   3 26  MOD2
Q12  2   2  1  MOD1
Q13 30   2  1  MOD3
Q14  1  17 22  MOD5 3
Q15 17  22 19  MOD2
Q16  1  15  9  MOD2
Q17 18   9 25  MOD2
Q18 17  20 21  MOD2
Q19 17  17 20  MOD2
Q20 26  21 23  MOD6 3
Q21 24  23 19  MOD1
Q22 15  24 26  MOD2
Q23 26  18 21  MOD1
Q24 24  24 26  MOD2
Q25 31   2  1  MOD4
R1  11  26 1K
R2  16  26 1K
R3  13  26 50K
R4   4  26 5K
R5  29   3 39K
R6  22  19 27
R7  19  23 27
R8  25  26 100
R9   9  26 50K
R10 20  21 40K
R11 24  26 50K
R12 14   5  1K
R13 19  14  93600K
R14 35   0  1K
C1  15  18 30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
VIN  5  0  DC  0.0
.DC VIN 0.0  0.0  0.0

*INDEPENDENT ZERO-VALUED INDEPENDENT VOLTAGE SOURCES
*SERVE AS AMMETERS IN THE CIRCUIT TO MONITOR VARIOUS
*TRANSISTOR COLLECTOR CURRENT VALUES

VM1    12  27
VM2    12  28
VM10    6  32
VM12    2  29
VM13   30  17
VM25   31  18
.PRINT DC V(19) V(14) I(VM1) I(VM2) I(VM10) I(VM12)
+I(VM13) I(VM25)
.END
```

APPENDIX H

PROGRAM FOR DETERMINING VOLTAGE AND CURRENT OFFSET OF BASIC MODEL

```
*****************************
*                           *
* LM741 INVERTING AMPLIFIER *
*                           *
*****************************
```

```
*THIS IS THE MODEL UTILIZED TO SIMULATE THE LM741 OP AMP
*IN A FINITE GAIN INVERTING AMPLIFIER CONFIGURATION;
*IT IS USED TO DETERMINE OFFSET VOLTAGE AND CURRENT

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

VCC  1  0     15
VEE 26  0    -15
Q1  12 27  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
R12 29  5  1K
R13 19 30  93600K
R14 28  0  1K
C1  15 18 30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
VIN  5  0  DC  0.0
.DC VIN 0.0  0.0  0.0

*INDEPENDENT ZERO-VALUED INDEPENDENT VOLTAGE SOURCES
*SERVE AS AMMETERS IN THE CIRCUIT

VM1    30  29
VM2    14  29
VM3    28  27
.PRINT DC V(19) V(14) V(27) I(VM1) I(VM2) I(VM3)
.END
```

APPENDIX I

PROGRAM FOR DETERMINING FREQUENCY RESPONSE FOR TWO CASCADE OA STAGES (K= -10)

```
*************************
*                       *
*  CASCADE AMPLIFIER    *
*                       *
*************************

*THIS CIRCUIT SIMULATES TWO CASCADED OPERATIONAL AMPLIFIER
*STAGES; IT IS UTILIZED TO DETERMINE FREQUENCY RESPONSE

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST STAGE AMPLIFIER

.SUBCKT OPAMP1 5,14,19
VCC  1  0     15
VEE 26  0    -15
Q1  12  5   8  MOD2
Q2  12 14   7  MOD2
Q3  10  6   8  MOD1
Q4  15  6   7  MOD1
Q5  10 13  11  MOD2
Q6  15 13  16  MOD2
Q7   1 10  13  MOD2
Q8  12 12   1  MOD1
Q9   6 12   1  MOD1
Q10  6  3   4  MOD2
Q11  3  3  26  MOD2
Q12  2  2   1  MOD1
Q13 17  2   1  MOD3
Q14  1 17  22  MOD5 3
Q15 17 22  19  MOD2
Q16  1 15   9  MOD2
Q17 18  9  25  MOD2
Q18 17 20  21  MOD2
Q19 17 17  20  MOD2
Q20 26 21  23  MOD6 3
Q21 24 23  19  MOD1
Q22 15 24  26  MOD2
Q23 26 18  21  MOD1
Q24 24 24  26  MOD2
Q25 18  2   1  MOD4
R1  11 26  1K
R2  16 26  1K
R3  13 26  50K
R4   4 26  5K
R5   2  3  39K
R6  22 19  27
R7  19 23  27
R8  25 26  100
R9   9 26  50K
R10 20 21  40K
R11 24 26  50K
C1  15 18  30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP1

*THIS DEFINES THE SECOND STAGE AMPLIFIER

.SUBCKT OPAMP2 5,14,19
VCC 1  0     15
VEE 26 0    -15
Q1  12  5   8  MOD2

Q2  12 14   7  MOD2
Q3  10  6   8  MOD1
Q4  15  6   7  MOD1
Q5  10 13  11  MOD2
Q6  15 13  16  MOD2
Q7   1 10  13  MOD2
Q8  12 12   1  MOD1
Q9   6 12   1  MOD1
Q10  6  3   4  MOD2
Q11  3  3  26  MOD2
Q12  2  2   1  MOD1
Q13 17  2   1  MOD3
Q14  1 17  22  MOD5 3
Q15 17 22  19  MOD2
Q16  1 15   9  MOD2
Q17 18  9  25  MOD2
Q18 17 20  21  MOD2
Q19 17 17  20  MOD2
Q20 26 21  23  MOD6 3
Q21 24 23  19  MOD1
Q22 15 24  26  MOD2
Q23 26 18  21  MOD1
Q24 24 24  26  MOD2
Q25 18  2   1  MOD4
R1  11 26  1K
R2  16 26  1K
R3  13 26  50K
R4   4 26  5K
R5   2  3  39K
R6  22 19  27
R7  19 23  27
R8  25 26  100
R9   9 26  50K
R10 20 21  40K
R11 24 26  50K
C1  15 18  30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP2
```

```
*DEFINE NOMINAL CIRCUIT
            *INSERT SUBCIRCUITS
X1    0    2    3    OPAMP1
X2    0    4    5    OPAMP2
            *BASIC CIRCUIT
R1    1    2    1K
R2    3    2    3162
R3    3    4    1K
R4    4    5    3162
VIN   1    0    AC    0.1
.AC   DEC   15   1   1MEG
.PRIIT  AC   VDB(5)
.PLOT AC VDB(5)
.END
```

APPENDIX J

PROGRAM FOR DETERMINING FREQUENCY RESPONSE FOR A C20A1 (K= -10)

```
***********************************
*                                 *
* COMPOSITE OPERATIONAL AMPLIFIER *
*             (C20A1)             *
*                                 *
***********************************


*THIS CIRCUIT SIMULATES A COMPOSITE OPERATIONAL AMPLIFIER
*(C20A1);IT IS UTILIZED TO DETERMINE FREQUENCY RESPONSE

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST OP AMP USED IN THE C20A1

.SUBCKT OPAMP1 5,14,19
VCC 1  0      15
VEE 26 0     -15
Q1   12  5  8  MOD2
Q2   12 14  7  MOD2
Q3   10  6  8  MOD1
Q4   15  6  7  MOD1
Q5   10 13 11  MOD2
Q6   15 13 16  MOD2
Q7    1 10 13  MOD2
Q8   12 12  1  MOD1
Q9    6 12  1  MOD1
Q10   6  3  4  MOD2
Q11   3  3 26  MOD2
Q12   2  2  1  MOD1
Q13  17  2  1  MOD3
Q14   1 17 22  MOD5 3
Q15  17 22 19  MOD2
Q16   1 15  9  MOD2
Q17  18  9 25  MOD2
Q18  17 20 21  MOD2
Q19  17 17 20  MOD2
Q20  26 21 23  MOD6 3
Q21  24 23 19  MOD1
Q22  15 24 26  MOD2
Q23  26 18 21  MOD1
Q24  24 24 26  MOD2
Q25  18  2  1  MOD4
R1   11 26 1K
R2   16 26 1K
R3   13 26 50K
R4    4 26 5K
R5    2  3 39K
R6   22 19 27
R7   19 23 27
R8   25 26 100
R9    9 26 50K
R10  20 21 40K
```

```
R11 24 26 50K
C1  15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP1

*THIS DEFINES THE SECCND OP AMP USED IN THE C2OA1

.SUBCKT OPAMP2 5,14,19
VCC 1  0    15
VEE 26 0    -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
C1  15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS CPAMP2
```

```
*DEFINE NCMINAL CIRCUIT
         *INSERT SUBCIRCUITS
X1   2   1   3    OPAMP1
X2   0   3   4    OPAMP2
         *BASIC CIRCUIT
R1   1   0   1K
R2   3   1   1.35K
R3   4   2   10K
R4   2   5   1K

VIN  5   0   AC     0.1
.AC  DEC 15  1 1MEG
.PRINT AC VDB(4)
.PLOT AC  VDB(4)

.END
```

APPENDIX K

PROGRAM FOR DETERMINING FREQUENCY RESPONSE FOR A C20A2 (K= -10)

```
*************************************
*  COMPOSITE OPERATIONAL AMPLIFIER  *
*              (C20A2)              *
*                                   *
*************************************


*THIS CIRCUIT SIMULATES A COMPOSITE OPERATIONAL AMPLIFIER
*(C20A2);IT IS UTILIZED TO DETERMINE FREQUENCY RESPONSE


.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7


**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST OP AMP USED IN THE C20A2

.SUBCKT OPAMP1 5,14,19
VCC 1  0      15
VEE 26 0     -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
C1  15 18 30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP1

*THIS DEFINES THE SECOND OP AMP USED IN THE C20A2

.SUBCKT OPAMP2 5,14,19
VCC 1  0     15
VEE 26 0    -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
C1  15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP2
```

```
*DEFINE NCMINAL CIRCUIT
         *INSERT SUBCIRCUITS
X1   0   1   2   OPAMP1
X2   2   3   4   OPAMP2
         *BASIC CIRCUIT
R1   3   0   1K
R2   3   4   1.35K
R3   4   1   10K
R4   1   5   1K

VIN  5   0   AC     0.1
.AC  DEC 15  1 1MEG
.PRINT AC VDB(4)
.PLOT AC  VDB(4)

.END
```

APPENDIX L

PROGRAM FOR DETERMINING FREQUENCY RESPONSE FOR A C20A3 (K= -10)

```
                        ************************************
                        *                                  *
                        *  COMPOSITE OPERATIONAL AMPLIFIER *
                        *              (C20A3)             *
                        *                                  *
                        ************************************


*THIS CIRCUIT SIMULATES A COMPOSITE OPERATIONAL AMPLIFIER
*(C20A3);IT IS UTILIZED TO DETERMINE FREQUENCY RESPONSE


.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7


**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST OP AMP USED IN THE C20A3

.SUBCKT CPAMP1 5,14,19
VCC  1  0      15
VEE  26 0     -15
Q1   12  5  8   MOD2
Q2   12 14  7   MOD2
Q3   10  6  8   MOD1
Q4   15  6  7   MOD1
Q5   10 13 11   MOD2
Q6   15 13 16   MOD2
Q7    1 10 13   MOD2
Q8   12 12  1   MOD1
Q9    6 12  1   MOD1
Q10   6  3  4   MOD2
Q11   3  3 26   MOD2
Q12   2  2  1   MOD1
Q13  17  2  1   MOD3
Q14   1 17 22   MOD5  3
Q15  17 22 19   MOD2
Q16   1 15  9   MOD2
Q17  18  9 25   MOD2
Q18  17 20 21   MOD2
Q19  17 17 20   MOD2
Q20  26 21 23   MOD6  3
Q21  24 23 19   MOD1
Q22  15 24 26   MOD2
Q23  26 18 21   MOD1
Q24  24 24 26   MOD2
Q25  18  2  1   MOD4
R1   11 26 1K
R2   16 26 1K
R3   13 26 50K
R4    4 26 5K
R5    2  3 39K
R6   22 19 27
R7   19 23 27
R8   25 26 100
R9    9 26 50K
R10  20 21 40K
```

```
R11  24  26  50K
C1   15  18  30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP1

*THIS DEFINES THE SECOND OP AMP USED IN THE C20A3

.SUBCKT OPAMP2 5,14,19
VCC  1   0     15
VEE  26  0    -15
Q1   12   5   8   MOD2
Q2   12  14   7   MOD2
Q3   10   6   8   MOD1
Q4   15   6   7   MOD1
Q5   10  13  11   MOD2
Q6   15  13  16   MOD2
Q7    1  10  13   MOD2
Q8   12  12   1   MOD1
Q9    6  12   1   MOD1
Q10   6   3   4   MOD2
Q11   3   3  26   MOD2
Q12   2   2   1   MOD1
Q13  17   2   1   MOD3
Q14   1  17  22   MOD5  3
Q15  17  22  19   MOD2
Q16   1  15   9   MOD2
Q17  18   9  25   MOD2
Q18  17  20  21   MOD2
Q19  17  17  20   MOD2
Q20  26  21  23   MOD6  3
Q21  24  23  19   MOD1
Q22  15  24  26   MOD2
Q23  26  18  21   MOD1
Q24  24  24  26   MOD2
Q25  18   2   1   MOD4
R1   11  26  1K
R2   16  26  1K
R3   13  26  50K
R4    4  26  5K
R5    2   3  39K
R6   22  19  27
R7   19  23  27
R8   25  26  100
R9    9  26  50K
R10  20  21  40K
R11  24  26  50K
C1   15  18  30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP2
```

```
*DEFINE NOMINAL CIRCUIT
         *INSERT SUBCIRCUITS
X1   1   4   3   OPAMP1
X2   2   4   5   OPAMP2
         *BASIC CIRCUIT
R1   4   2   1K
R2   3   2   4K
R3   4   5   10K
R4   6   4   1K
R5   1   0   1K
VIN  6   0   AC    0.1
.AC  DEC 15  1 1MEG
.PRINT AC VDB(5)
.PLOT AC  VDB(5)

.END
```

APPENDIX M

PROGRAM FOR DETERMINING FREQUENCY RESPONSE FOR A C20A4 (K= -10)

```
                *************************************
                *                                   *
                *  COMPOSITE OPERATIONAL AMPLIFIER  *
                *              (C20A4)              *
                *                                   *
                *************************************


*THIS CIRCUIT SIMULATES A COMPOSITE OPERATIONAL AMPLIFIER
*(C20A4);IT IS UTILIZED TO DETERMINE FREQUENCY RESPONSE


.WIDTH  IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7


**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST OP AMP USED IN THE C20A4

.SUBCKT OPAMP1 5,14,19
VCC  1  0     15
VEE 26  0    -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
C1  15 18 30P
```

```
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MCD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP1

*THIS DEFINES THE SECOND OP AMP USED IN THE C20A4

.SUBCKT OPAMP2 5,14,19
VCC 1  0     15
VEE 26 0    -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5  3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6  3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
C1  15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP2
```

```
*DEFINE NOMINAL CIRCUIT
          *INSERT SUBCIRCUITS
X1    0   1   2   OPAMP1
X2    3   1   4   OPAMP2
          *BASIC CIRCUIT
R1    3   0   1K
R2    3   2   2K
R3    4   1   10K
R4    5   1   1K
VIN   5   0   AC     0.1
.AC   DEC 15  1 1MEG
.PRINT AC VDB(4)
.PLOT AC  VDB(4)

.END
```

APPENDIX N

PROGRAM FOR DETERMINING SLEW RATE OF A C20A1

```
                         ********************************
                         *                              *
                         *   C20A1 INVERTING AMPLIFIER  *
                         *                              *
                         ********************************


*THIS CIRCUIT SIMULATES A C20A1 INVERTING AMPLIFIER

*IT IS UTILIZED TO TEST THE EFFECTS OF COMBINING A FAST
*SLEW RATE OP AMP WITH A SLOWER SLEW RATE OP AMP;
*IN ITS PRESENT CONFIGURATION THE C20A1 HAS THE FAST OA
*AS THE FIRST OA AND THE SLOW OA AS THE SECOND OA;THE
*SPEED OF EITHER OA IS ADJUSTED BY ADJUSTING THE VALUE
*OF THE COMPENSATING CAPACITOR

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST OP AMP USED IN THE C20A1

.SUBCKT OPAMP1 5,14,19
VCC 1  0     15
VEE 26 0    -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD2 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD1 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
```

```
R6   22 19 27
R7   19 23 27
R8   25 26 100
R9    9 26 50K
R10  20 21 40K
R11  24 26 50K
C1   15 18 10P
.MODEL MOD1 PNP(BF=50 IS=10F)
.MODEL MOD2 NPN(BF=200 IS=10F)
.MODEL MOD3 PNP(BF=50 IS=2.5F)
.MODEL MOD4 PNP(BF=50 IS=7.5F)
.ENDS OPAMP1

*THIS DEFINES THE SECOND OP AMP USED IN THE C20A1

.SUBCKT OPAMP2 5,14,19
VCC 1  0     15
VEE 26 0    -15
Q1   12  5  8  MOD2
Q2   12 14  7  MOD2
Q3   10  6  8  MOD1
Q4   15  6  7  MOD1
Q5   10 13 11  MOD2
Q6   15 13 16  MOD2
Q7    1 10 13  MOD2
Q8   12 12  1  MOD1
Q9    6 12  1  MOD1
Q10   6  3  4  MOD2
Q11   3  3 26  MOD2
Q12   2  2  1  MOD1
Q13  17  2  1  MOD3
Q14   1 17 22  MOD2 3
Q15  17 22 19  MOD2
Q16   1 15  9  MOD2
Q17  18  9 25  MOD2
Q18  17 20 21  MOD2
Q19  17 17 20  MOD2
Q20  26 21 23  MOD1 3
Q21  24 23 19  MOD1
Q22  15 24 26  MOD2
Q23  26 18 21  MOD1
Q24  24 24 26  MOD2
Q25  18  2  1  MOD4
R1   11 26 1K
R2   16 26 1K
R3   13 26 50K
R4    4 26 5K
R5    2  3 39K
R6   22 19 27
R7   19 23 27
R8   25 26 100
R9    9 26 50K
R10  20 21 40K
R11  24 26 50K
C1   15 18 30P
```

```
.MODEL MOD1 PNP(BF=50  IS=10F)
.MODEL MOD2 NPN(BF=200 IS=10F)
.MODEL MOD3 PNP(BF=50 IS=2.5F)
.MODEL MOD4 PNP(BF=50 IS=7.5F)
.ENDS OPAMP2

*DEFINE NOMINAL CIRCUIT;C20A1 NON-INVERTING AMPLIFIER
         *INSERT SUBCIRCUITS
X1   2   1   3   OPAMP1
X2   0   3   4   OPAMP2
R1   1   0   1K
R2   3   1   1K
R3   4   2   1K
R4   2   5   1K
VIN  5  0  PULSE(5.0  -5.0 10US 5NS 5NS 60US 120US)
.TRAN 1US  95US
.PRINT TRAN V(4)
.PLOT  TRAN V(4)
.END
```

APPENDIX O

PROGRAM FOR DETERMINING OFFSET OF C20A3

```
                 ***********************************
                 *                                 *
                 *  C20A3 NON-INVERTING AMPLIFIER  *
                 *                                 *
                 ***********************************


*THIS CIRCUIT SIMULATES A C20A3 NON-INVERTING AMPLIFIER

*IT IS UTILIZED TO TEST THE EFFECTS OF COMBINING A POOR
*OFFSET OA WITH A BETTER OFFSET OA

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7


**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST OP AMP USED IN THE C20A3

.SUBCKT OPAMP1 5,14,19
VCC 1  0     15
VEE 26 0    -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD2 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD1 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
```

```
R11 24 26 50K
C1  15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F)
.MODEL MOD2 NPN(BF=200 IS=10F)
.MODEL MOD3 PNP(BF=50 IS=2.5F)
.MODEL MOD4 PNP(BF=50 IS=7.5F)
.ENDS OPAMP1

*THIS DEFINES THE SECOND OP AMP USED IN THE C20A3

.SUBCKT OPAMP2 5,14,19
VCC 1  0     15
VEE 26 0    -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6 28  MOD1
Q4  15  6 29  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD2 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD1 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
RE1  8 28 10K
RE2  7 29 10.05K
C1  15 18 30P
.MODEL MOD1 PNP(BF=50  IS=10F)
.MODEL MOD2 NPN(BF=200 IS=10F)
.MODEL MOD3 PNP(BF=50 IS=2.5F)
.MODEL MOD4 PNP(BF=50 IS=7.5F)
.ENDS OPAMP2
```

```
*DEFINE NOMINAL CIRCUIT;C20A3 NON-INVERTING AMPLIFIER
        *INSERT SUBCIRCUITS
X1  1   2   3  OPAMP2
X2  4   2   5  OPAMP1
R1  4   2   1K
R2  3   4   2K
R3  5   2   50K
R4  2   0   1K
VIN 1  0  0.5
.DC VIN     -.8    .8     .01
.PRINT  DC V(5) V(1) V(2)
.PLOT   DC V(5)
.END
```

APPENDIX P

PROGRAM FOR FREQUENCY RESPONSE OF MFB BIQUAD (SINGLE OA)

```
                 ****************************
                 *                          *
                 * MULTIPLE FEEDBACK FILTER *
                 *                          *
                 ****************************

*THIS CIRCUIT SIMULATES A MULTIPLE FEEDBACK SINGLE-BIQUAD
*FILTER

*IT MAY SIMULATE THE FILTER AS A SINGLE OP-AMP OR A
*COMPOSITE OP AMP WITH N=2 BY ADJUSTING THE NOMINAL
*CIRCUIT


.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7


**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST OP-AMP USED IN THE C2OA

.SUBCKT OPAMP1 5,14,19
VCC  1   0     15
VEE  26  0    -15
Q1   12   5   8   MOD2
Q2   12  14   7   MOD2
Q3   10   6   8   MOD1
Q4   15   6   7   MOD1
Q5   10  13  11   MOD2
Q6   15  13  16   MOD2
Q7    1  10  13   MOD2
Q8   12  12   1   MOD1
Q9    6  12   1   MOD1
Q10   6   3   4   MOD2
Q11   3   3  26   MOD2
Q12   2   2   1   MOD1
Q13  17   2   1   MOD3
Q14   1  17  22   MOD5 3
Q15  17  22  19   MOD2
Q16   1  15   9   MOD2
Q17  18   9  25   MOD2
Q18  17  20  21   MOD2
Q19  17  17  20   MOD2
Q20  26  21  23   MOD6 3
Q21  24  23  19   MOD1
Q22  15  24  26   MOD2
Q23  26  18  21   MOD1
Q24  24  24  26   MOD2
Q25  18   2   1   MOD4
R1   11  26  1K
R2   16  26  1K
R3   13  26  50K
R4    4  26  5K
R5    2   3  39K
R6   22  19  27
R7   19  23  27
```

```
R8   25 26 100
R9    9 26 50K
R10 20 21 40K
R11 24 26 50K
C1   15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP1
.SUBCKT OPAMP2 5,14,19
VCC 1  0     15
VEE 26 0    -15
Q1   12  5  8  MOD2
Q2   12 14  7  MOD2
Q3   10  6  8  MOD1
Q4   15  6  7  MOD1
Q5   10 13 11  MOD2
Q6   15 13 16  MOD2
Q7    1 10 13  MOD2
Q8   12 12  1  MOD1
Q9    6 12  1  MOD1
Q10   6  3  4  MOD2
Q11   3  3 26  MOD2
Q12   2  2  1  MOD1
Q13  17  2  1  MOD3
Q14   1 17 22  MOD5 3
Q15  17 22 19  MOD2
Q16   1 15  9  MOD2
Q17  18  9 25  MOD2
Q18  17 20 21  MOD2
Q19  17 17 20  MOD2
Q20  26 21 23  MOD6 3
Q21  24 23 19  MOD1
Q22  15 24 26  MOD2
Q23  26 18 21  MOD1
Q24  24 24 26  MOD2
Q25  18  2  1  MOD4
R1   11 26 1K
R2   16 26 1K
R3   13 26 50K
R4    4 26 5K
R5    2  3 39K
R6   22 19 27
R7   19 23 27
R8   25 26 100
R9    9 26 50K
R10  20 21 40K
R11  24 26 50K
C1   15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP2
```

```
*DEFINE NOMINAL CIRCUIT;BP FILTER W/LM741
         *INSERT SUBCIRCUITS
X1   0   4   5   OPAMP1
*2   0   7   5   OPAMP2
         *BASIC CIRCUIT
R1   1   2   100
R2   3   4   100
R3   4   5   2.4K
C1   2   5   7.96N
C2   2   3   7.96N
VIN  1   0    AC  0.1
.AC  DEC 175 20K  60K

.PRINT AC VDB(5)
.PLOT AC VDB(5)

.END
```

APPENDIX Q

PROGRAM FOR FREQUENCY RESPONSE OF MFB BIQUAD (C20A1)

```
***************************************
*                                     *
*  MULTIPLE FEEDBACK BANDPASS FILTER  *
*                                     *
***************************************


*THIS CIRCUIT SIMULATES A MULTIPLE FEEDBACK SINGLE-BIQUAD
*FILTER;IT MAY SIMULATE THE FILTER AS A SINGLE OP AMP OR
*AS A COMPOSITE OP AMP WITH N=2 BY ADJUSTING THE NOMINAL
*CIRCUIT;IN ITS CURRENT CONFIGURATION IT IS USING C20A1'S

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7

**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST OP AMP USED IN THE C20A1

.SUBCKT OPAMP1 5,14,19
VCC  1  0    15
VEE 26  0   -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
```

```
R10 20 21 40K
R11 24 26 50K
C1  15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP1

*THIS DEFINES THE SECCND OP AMP USED IN THE C20A1

.SUBCKT OPAMP2 5,14,19
VCC 1  0     15
VEE 26 0    -15
Q1  12  5  8  MOD2
Q2  12 14  7  MOD2
Q3  10  6  8  MOD1
Q4  15  6  7  MOD1
Q5  10 13 11  MOD2
Q6  15 13 16  MOD2
Q7   1 10 13  MOD2
Q8  12 12  1  MOD1
Q9   6 12  1  MOD1
Q10  6  3  4  MOD2
Q11  3  3 26  MOD2
Q12  2  2  1  MOD1
Q13 17  2  1  MOD3
Q14  1 17 22  MOD5 3
Q15 17 22 19  MOD2
Q16  1 15  9  MOD2
Q17 18  9 25  MOD2
Q18 17 20 21  MOD2
Q19 17 17 20  MOD2
Q20 26 21 23  MOD6 3
Q21 24 23 19  MOD1
Q22 15 24 26  MOD2
Q23 26 18 21  MOD1
Q24 24 24 26  MOD2
Q25 18  2  1  MOD4
R1  11 26 1K
R2  16 26 1K
R3  13 26 50K
R4   4 26 5K
R5   2  3 39K
R6  22 19 27
R7  19 23 27
R8  25 26 100
R9   9 26 50K
R10 20 21 40K
R11 24 26 50K
C1  15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP2
```

```
*DEFINE NCMINAL CIRCUIT;BP FILTER W/C20A1
          *INSERT SUBCIRCUITS
X1    4    6    7    OPAMP1
X2    0    7    5    OPAMP2
          *BASIC CIRCUIT
R1    1    2    100
R2    3    4    100
R3    4    5    2.4K
C1    2    5    7.96N
C2    2    3    7.96N
R4    0    6    1K
R5    6    7    15.75K
VIN   1    0     AC   0.1
.AC   DEC 175 10K   60K

.PRINT AC VDB(5)
.PLOT AC VDB(5)

.END
```

APPENDIX R

PROGRAM FOR FREQUENCY RESPONSE OF MFB BIQUAD (IDEAL OA'S)

```
$JOB
C                *********************
C                *                   *
C                * IDEAL MFB FILTER  *
C                *                   *
C                *********************

C     THIS PROGRAM DETERMINES THE FREQUENCY RESPONSE
C     OF A MULTIPLE FEEDBACK FILTER USING IDEAL OA'S

      DOUBLE PRECISION AX(100),AY(100),AZ(100)
      COMPLEX  FF,S
      GAIN=24.
      Y=2.E-6
      OM=0.0
      DO 20 K=1,100
           OM=OM+2000.
           AX(K)=OM
           S=CMPLX(0.0,OM)
           FF=((-GAIN)*S*Y)/(1.+(3.*S*Y)+(S*S*Y*Y*
     *     (GAIN+1.)))*0.1
           AZ(K)=20.0*ALOG10(CABS(FF))
           AR=REAL(FF)
           AI=AIMAG(FF)
           AY(K)=ATAN2(AI,AR)
           wRITE(6,100) AX(K),AY(K),AZ(K)
20         CONTINUE
100        FORMAT(5X,E14.7,4X,F14.7,4X,F14.7)
           STOP
           END
$ENTRY
```

APPENDIX S

PROGRAM FOR FREQUENCY RESPONSE OF GIC BP FILTER USING A C20A4 AND A C20A3

```
                              ***********************
                              *                     *
                              * GIC BANDPASS FILTER *
                              *                     *
                              ***********************


*THIS CIRCUIT SIMULATES A BP GIC FILTER USING C20A'S

*IT MAY SIMULATE THE FILTER AS A SINGLE OP-AMP OR A
*COMPOSITE OP AMP WITH N=2 BY ADJUSTING THE NOMINAL
*CIRCUIT;IN ITS CURRENT CONFIGURATION IT IS USING
*A C20A4 AND A C20A3

.WIDTH IN=80 OUT=80
.OPT ACCT LIST NODE LVLCOD=2  LIMPTS=1200 NUMDGT=7


**SUBCIRCUIT DEFINITION

*THIS DEFINES THE FIRST OP AMP USED IN THE C20A

.SUBCKT OPAMP1 5,14,19
VCC  1  0      15
VEE  26 0     -15
Q1   12  5  8  MOD2
Q2   12 14  7  MOD2
Q3   10  6  8  MOD1
Q4   15  6  7  MOD1
Q5   10 13 11  MOD2
Q6   15 13 16  MOD2
Q7    1 10 13  MOD2
Q8   12 12  1  MOD1
Q9    6 12  1  MOD1
Q10   6  3  4  MOD2
Q11   3  3 26  MOD2
Q12   2  2  1  MOD1
Q13  17  2  1  MOD3
Q14   1 17 22  MOD5 3
Q15  17 22 19  MOD2
Q16   1 15  9  MOD2
Q17  18  9 25  MOD2
Q18  17 20 21  MOD2
Q19  17 17 20  MOD2
Q20  26 21 23  MOD6 3
Q21  24 23 19  MOD1
Q22  15 24 26  MOD2
Q23  26 18 21  MOD1
Q24  24 24 26  MOD2
Q25  18  2  1  MOD4
R1   11 26 1K
R2   16 26 1K
R3   13 26 50K
R4    4 26 5K
R5    2  3 39K
R6   22 19 27
R7   19 23 27
R8   25 26 100
```

```
R9    9 26 50K
R10  20 21 40K
R11  24 26 50K
C1   15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP1

*THIS DEFINES THE SECOND OP AMP USED IN THE C20A

.SUBCKT OPAMP2 5,14,19
VCC   1  0     15
VEE  26  0    -15
Q1   12  5  8  MOD2
Q2   12 14  7  MOD2
Q3   10  6  8  MOD1
Q4   15  6  7  MOD1
Q5   10 13 11  MOD2
Q6   15 13 16  MOD2
Q7    1 10 13  MOD2
Q8   12 12  1  MOD1
Q9    6 12  1  MOD1
Q10   6  3  4  MOD2
Q11   3  3 26  MOD2
Q12   2  2  1  MOD1
Q13  17  2  1  MOD3
Q14   1 17 22  MOD5 3
Q15  17 22 19  MOD2
Q16   1 15  9  MOD2
Q17  18  9 25  MOD2
Q18  17 20 21  MOD2
Q19  17 17 20  MOD2
Q20  26 21 23  MOD6 3
Q21  24 23 19  MOD1
Q22  15 24 26  MOD2
Q23  26 18 21  MOD1
Q24  24 24 26  MOD2
Q25  18  2  1  MOD4
R1   11 26 1K
R2   16 26 1K
R3   13 26 50K
R4    4 26 5K
R5    2  3 39K
R6   22 19 27
R7   19 23 27
R8   25 26 100
R9    9 26 50K
R10  20 21 40K
R11  24 26 50K
C1   15 18 30P
.MODEL MOD1 PNP(BF=50 IS=10F CJE=0.1P CJC=1.05P CJS=5.1P)
.MODEL MOD2 NPN(BF=200 IS=10F CJE=0.65P CJC=0.36P CJS=3.2P)
.MODEL MOD3 PNP(BF=50 IS=2.5F CJE=0.1P CJC=0.3P CJS=4.8P)
.MODEL MOD4 PNP(BF=50 IS=7.5F CJE=0.1P CJC=0.9P CJS=4.8P)
.MODEL MOD5 NPN(BF=200 IS=10F CJE=2.8P CJC=1.55P CJS=7.8P)
.MODEL MOD6 PNP(BF=50 IS=10F CJE=4.05P CJC=2.8P)
.ENDS OPAMP2
```

```
*DEFINE NOMINAL CIRCUIT;BP FILTER W/C20A4 AND C20A3
          *INSERT SUBCIRCUITS
X1    3    2    9    OPAMP1
X2    4    2    6    OPAMP1
X3    7    2   10    OPAMP1
X4    8    2    5    OPAMP1
          *BASIC CIRCUIT
R1    5    2    100
R2    5    3    100
R4    6    7    100
R6    3    0    100
R7    1    7    1K
R8    9    4    150
R9    3    4    1K
R10   10   8    13.8K
R11   2    8    1K
C3    6    2    79.58N
C8    7    0    79.58N
VIN   1    0     AC   1.0
.AC   DEC 175   5K   35K

.PRINT AC VDB(5)
.PLOT AC VDB(5)

.END
```

APPENDIX T

PROGRAM FOR FREQUENCY RESPONSE OF GIC BP FILTER (IDEAL OA'S)

```
$JOB
C                          **********************
C                          *                    *
C                          * IDEAL GIC FILTER   *
C                          *                    *
C                          **********************


C        THIS PROGRAM DETERMINES THE FREQUENCY RESPONSE
C        OF A GIC FILTER USING IDEAL OA'S
      DIMENSION AY(100),AX(100),AZ(100)
      COMPLEX FF,S,UP,DD
C     Y=1/GBWP
      Y = 0.
      G1 = .215E-3
      G2 = G1
      G4 = G1
      G5 = 0.
      G6 = G1
C     *G7 AND C3 DETERMINE FO
      G7 = .215E-4
      C3 = 1.71E-9
      C8 = C3
      A1 = 2.
      A2 = 2.
      OMEGA = 6.283E+4
      DO 20 K = 1,100
      OMEGA = OMEGA + 1256.64
      AX(K) = OMEGA
      S = CMPLX(0.0,OMEGA)
      AA1 =G7*C3
      AA2 =A1*G1*G7*Y*Y+A1*G7*C3*Y
      AA3 =A1*G7*C3*Y*Y
      BB0 =G1*G4*G6/(G2+G6)
      BB1 =G2*G7*C3/(G2+G6)+(A1-1.)*G1*G4*G6*Y/(G2+G6)+
     *    G1*G4*Y
      BB2 =G2*C3*C8/(G2+G6)+(A1-1.)*G2*G7*C3*Y/(G2+G6)+
     * G2*(G4+G7)*C3*Y/(G2+G6)+A1*G1*(G4+G7)*Y*Y
      BB3 =A1*G2*C3*C8*Y/(G2+G6)+A2*(G4+G7)*C3*Y*Y+A1*
     *    G1*C8*Y*Y+
     * (A1-1.)*G2*(G4+G7)*C3*Y*Y/(G2+G6)+A1*G1*(G4+G7)*
     *  Y**3
      BB4 =A2*C3*C8*Y*Y+(A1-1.)*G2*C3*C8*Y*Y/(G2+G6)+
     * A1*A2*(G4+G7)*C3*Y**3+A1*G1*C8*Y**3+A1*A2*G1*
     *    (G4+G7)*Y**4
      BB5 =A1*A2*C3*C8*Y**3+A1*A2*(G4+G7)*C3*Y**4+A1*
     *     A2*G1*C8*Y**4
      BB6 =A1*A2*C3*C8*Y**4
      UP = S*AA1 + S*S*AA2 + S**3*AA3
      DD = BB0 + S*BB1 + S*S*BB2 + S**3*BB3 + S**4*BB4
     *     + S**5*BB5+
     * S**6*BB6
      FF =(UP / DD)*1.0
      AZ(K) = 20.*ALOG10(CABS(FF))
      AR = REAL(FF)
      AI = AIMAG(FF)
      AY(K) = ATAN2(AI,AR)
      AX(K) = AX(K)/(2.*3.1416)
      WRITE(6,66) AX(K), AY(K),AZ(K)
20    CONTINUE
   66 FORMAT(5X,E14.5,5X,F14.5,5X,F14.5)
      STOP
      END
$ENTRY
```

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9.	Prof Mitchell Cotton, Code 62Cc Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5100	1

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